FIG. 1

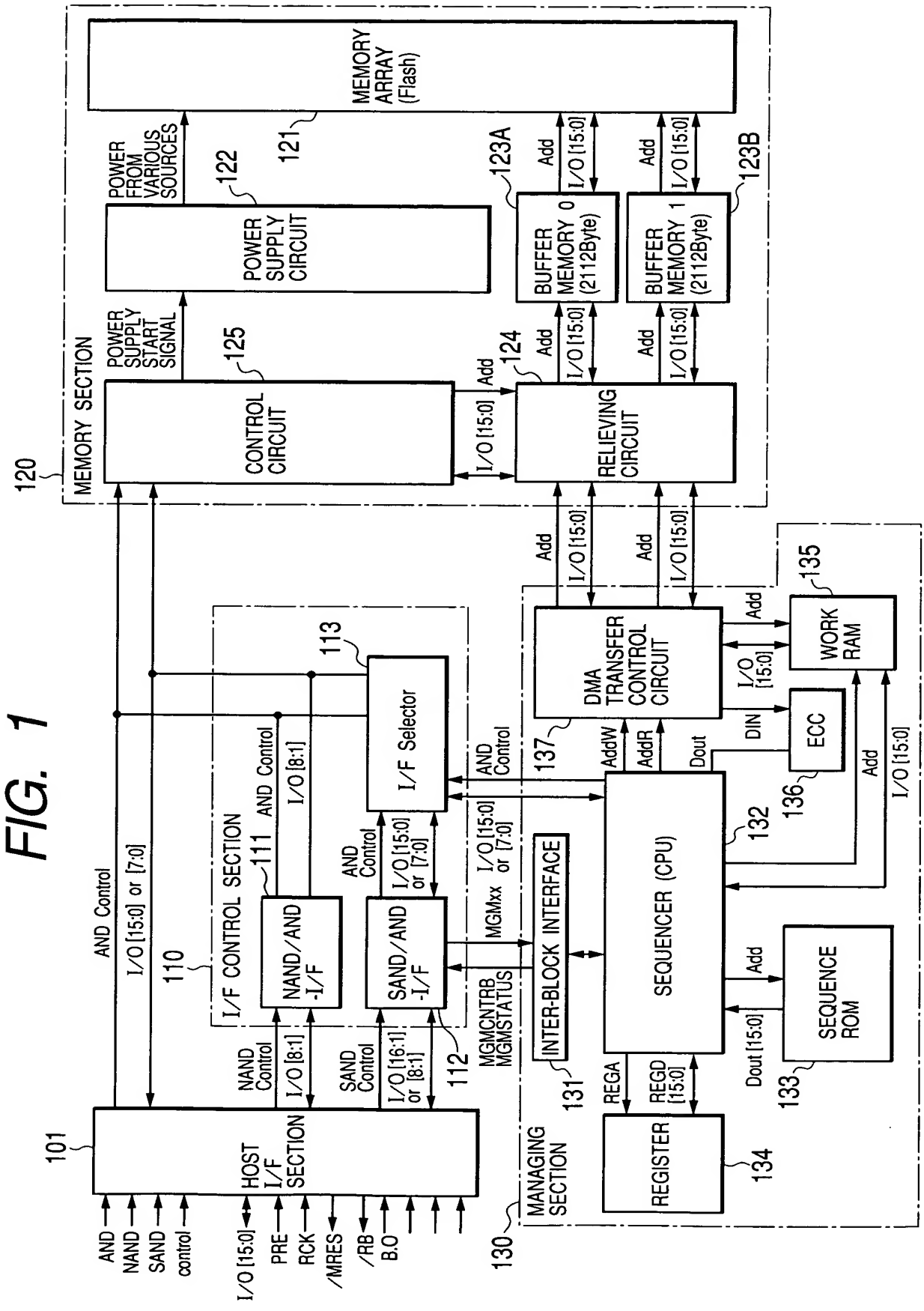

MEMORY SECTION
120
MEMORY ARRAY (Flash)
121
POWER FROM VARIOUS SOURCES
122
POWER SUPPLY CIRCUIT
123A
BUFFER MEMORY 0 (2112Byte)
123B
BUFFER MEMORY 1 (2112Byte)
124
RELIEVING CIRCUIT
125
CONTROL CIRCUIT
POWER SUPPLY START SIGNAL
Add
I/O [15:0]
MANAGING SECTION
130
DMA TRANSFER CONTROL CIRCUIT
135
WORK RAM
137
AddW
AddR
Dout
DIN
ECC
136
132
SEQUENCER (CPU)
INTER-BLOCK INTERFACE
131
REGA
REGD [15:0]
REGISTER
134
Dout [15:0]
SEQUENCE ROM
133
I/F CONTROL SECTION
110
I/F Selector
113
AND Control
I/O [15:0] or [7:0]
111
NAND/AND -I/F
SAND/AND -I/F
112
MGMxx
MGMCNTRB
MGMSTATUS
NAND Control
SAND Control
I/O [8:1]
I/O [16:1] or [8:1]
HOST I/F SECTION
101
AND
NAND
SAND
control
PRE
RCK
/MRES
/RB
B.O

FIG. 2

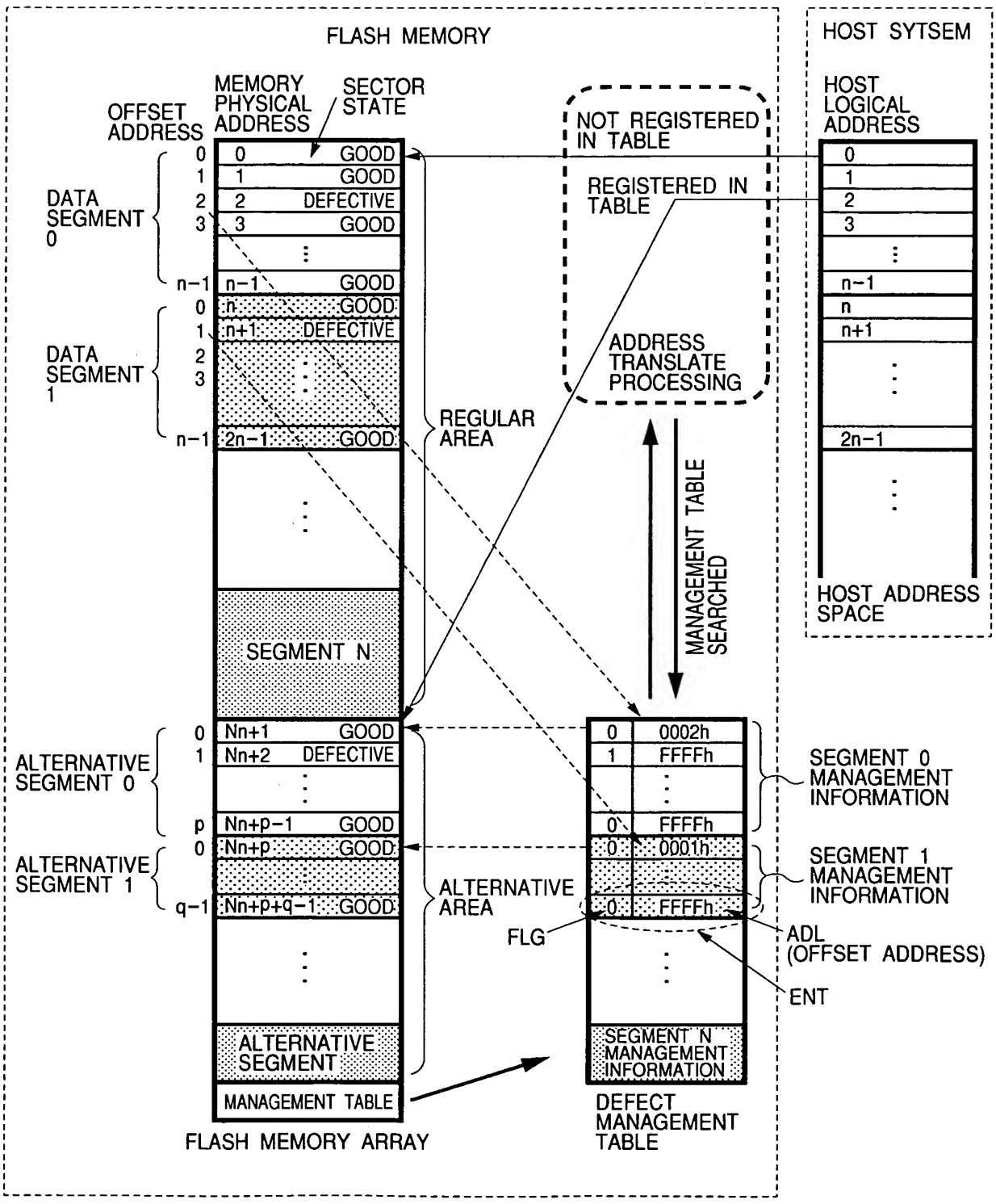

FLASH MEMORY
HOST SYTSEM
MEMORY PHYSICAL ADDRESS
SECTOR STATE
OFFSET ADDRESS
HOST LOGICAL ADDRESS
NOT REGISTERED IN TABLE
REGISTERED IN TABLE
DATA SEGMENT 0
DATA SEGMENT 1
ADDRESS TRANSLATE PROCESSING
REGULAR AREA
MANAGEMENT TABLE SEARCHED
SEGMENT N
HOST ADDRESS SPACE
ALTERNATIVE SEGMENT 0
ALTERNATIVE SEGMENT 1
ALTERNATIVE AREA
SEGMENT 0 MANAGEMENT INFORMATION
SEGMENT 1 MANAGEMENT INFORMATION
FLG
ADL (OFFSET ADDRESS)
ENT
ALTERNATIVE SEGMENT
MANAGEMENT TABLE
SEGMENT N MANAGEMENT INFORMATION
FLASH MEMORY ARRAY
DEFECT MANAGEMENT TABLE

FIG. 3

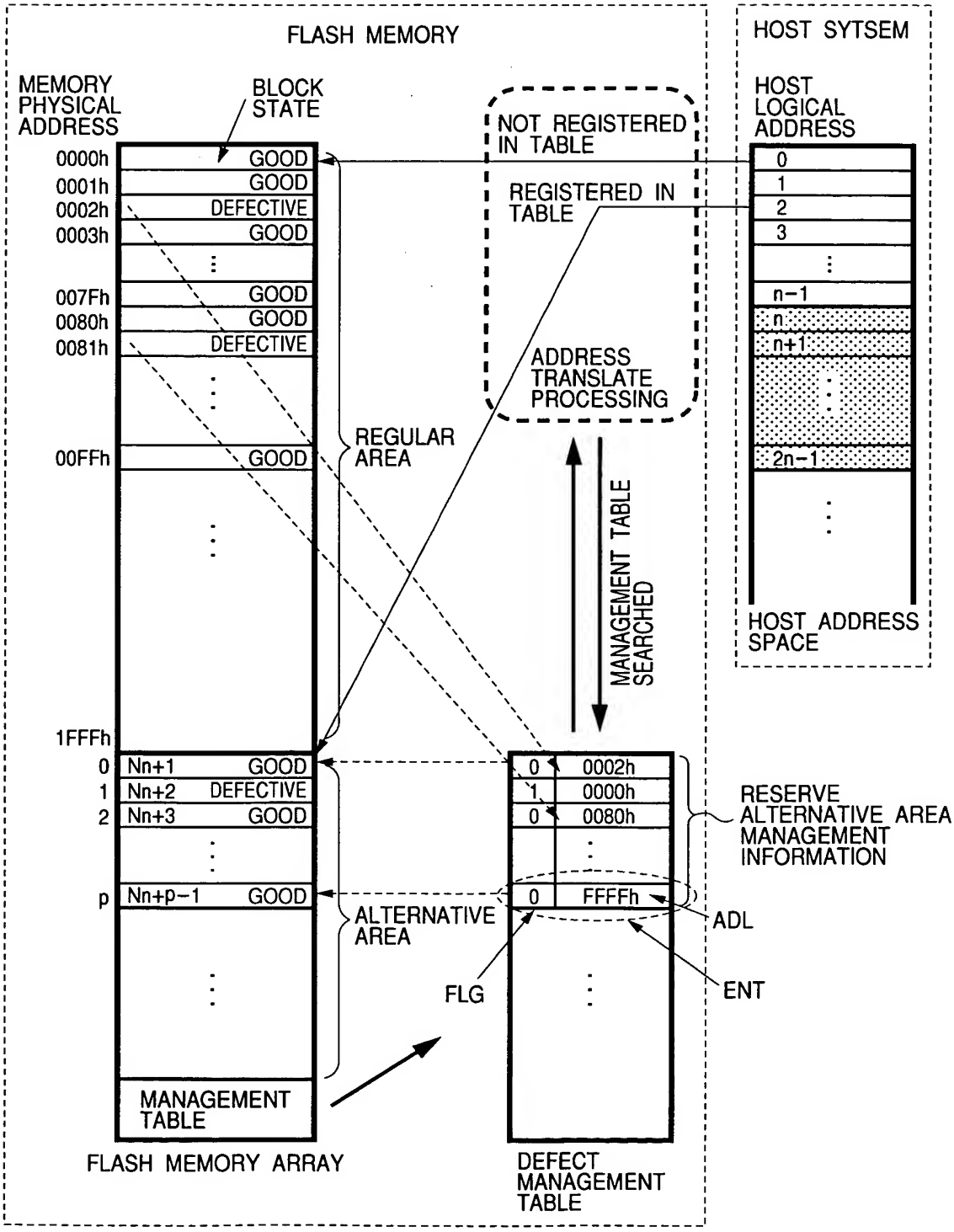

FLASH MEMORY
HOST SYTSEM
MEMORY PHYSICAL ADDRESS
BLOCK STATE
HOST LOGICAL ADDRESS
NOT REGISTERED IN TABLE
REGISTERED IN TABLE
ADDRESS TRANSLATE PROCESSING
REGULAR AREA
MANAGEMENT TABLE SEARCHED
HOST ADDRESS SPACE
0000h GOOD
0001h GOOD
0002h DEFECTIVE
0003h GOOD
007Fh GOOD
0080h GOOD
0081h DEFECTIVE
00FFh GOOD
1FFFh
0 Nn+1 GOOD
1 Nn+2 DEFECTIVE
2 Nn+3 GOOD
p Nn+p−1 GOOD
ALTERNATIVE AREA
MANAGEMENT TABLE
FLASH MEMORY ARRAY
0 0002h
1 0000h
0 0080h
0 FFFFh
RESERVE ALTERNATIVE AREA MANAGEMENT INFORMATION
ADL
ENT
FLG
DEFECT MANAGEMENT TABLE

FIG. 4

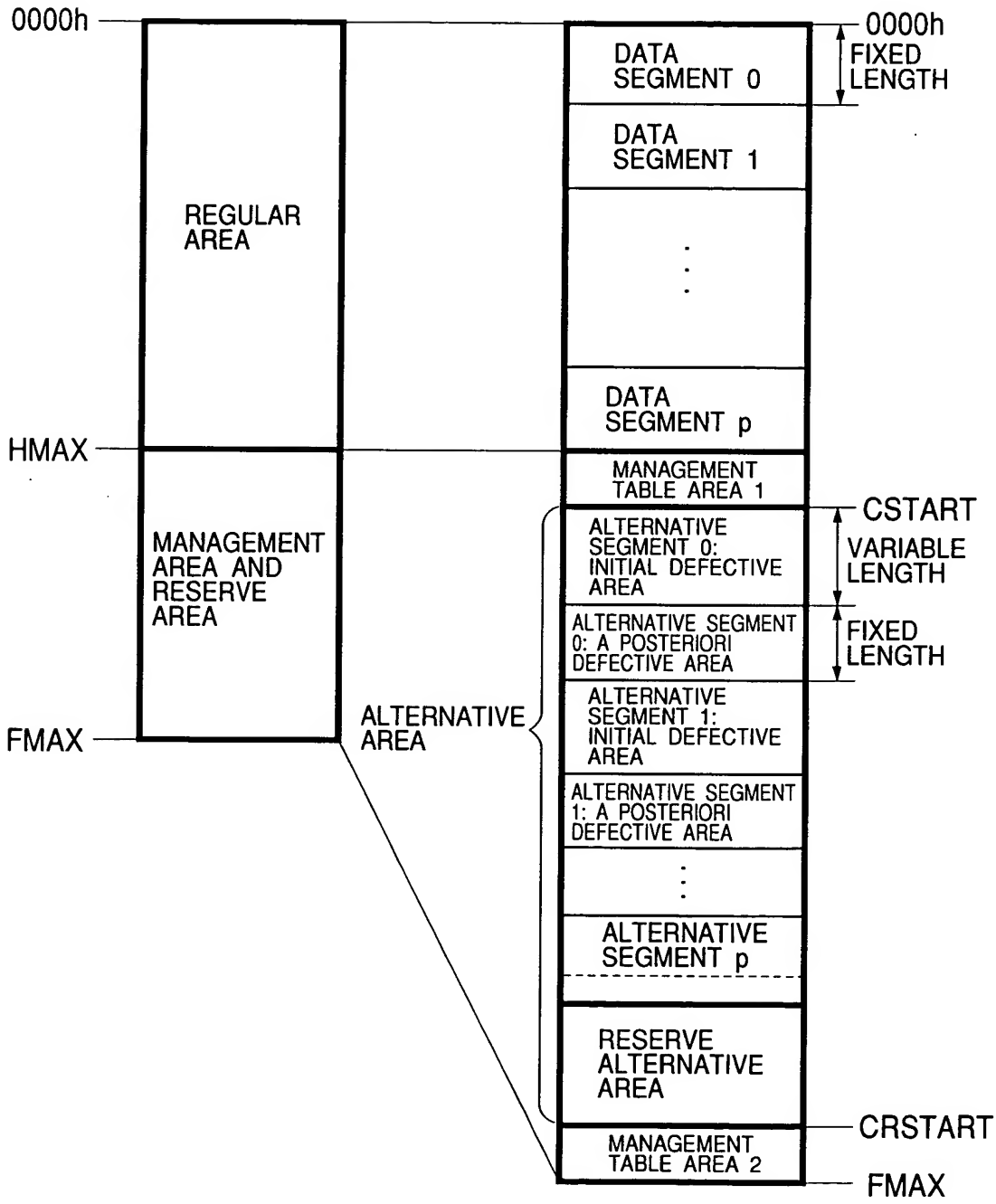

0000h
HMAX
FMAX
REGULAR AREA
MANAGEMENT AREA AND RESERVE AREA
ALTERNATIVE AREA
DATA SEGMENT 0
DATA SEGMENT 1
DATA SEGMENT p
MANAGEMENT TABLE AREA 1
ALTERNATIVE SEGMENT 0: INITIAL DEFECTIVE AREA
ALTERNATIVE SEGMENT 0: A POSTERIORI DEFECTIVE AREA
ALTERNATIVE SEGMENT 1: INITIAL DEFECTIVE AREA
ALTERNATIVE SEGMENT 1: A POSTERIORI DEFECTIVE AREA
ALTERNATIVE SEGMENT p
RESERVE ALTERNATIVE AREA
MANAGEMENT TABLE AREA 2
0000h
FIXED LENGTH
CSTART
VARIABLE LENGTH
FIXED LENGTH
CRSTART
FMAX

FIG. 5

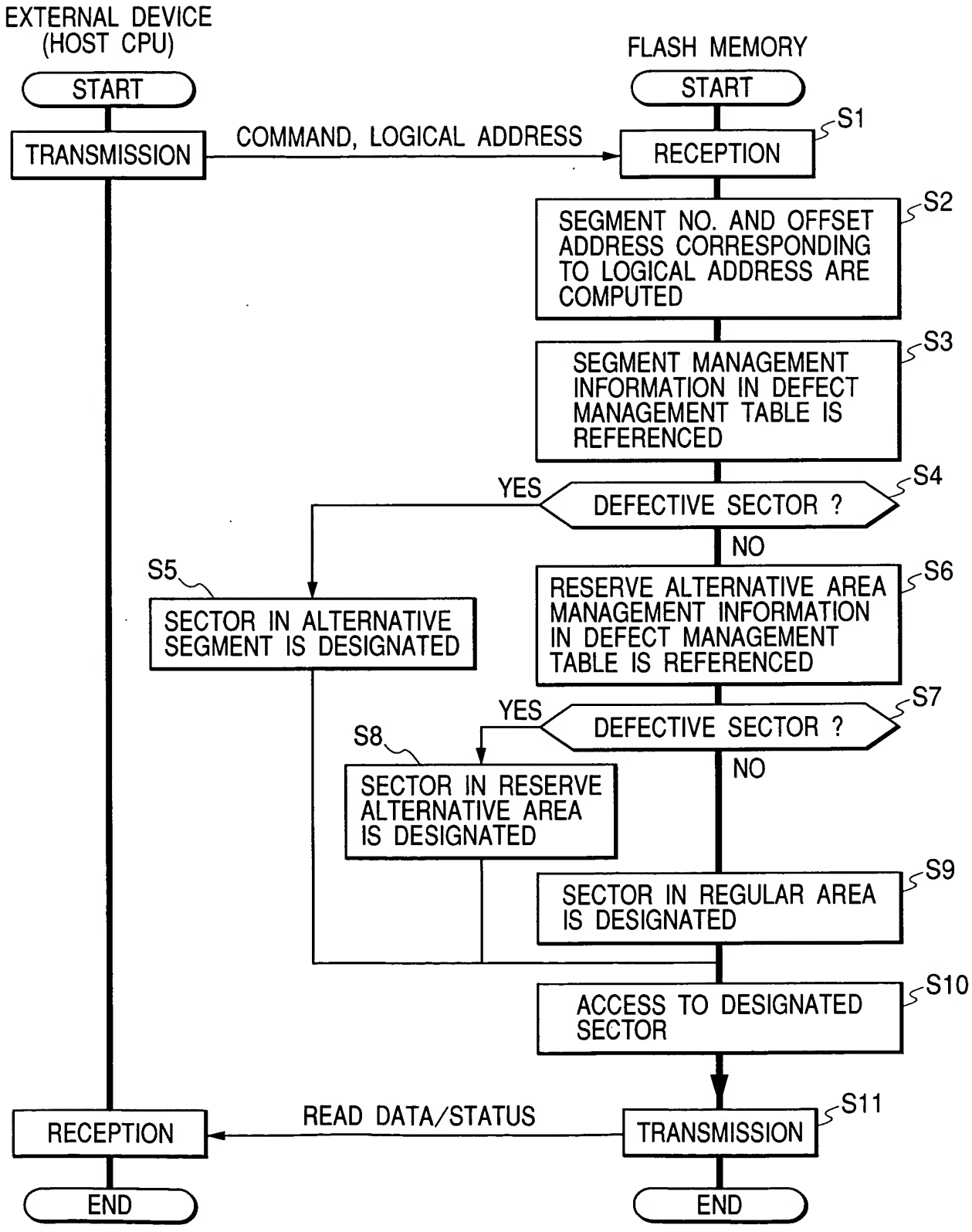

EXTERNAL DEVICE
(HOST CPU)
FLASH MEMORY
START
START
TRANSMISSION
COMMAND, LOGICAL ADDRESS
RECEPTION
S1
SEGMENT NO. AND OFFSET ADDRESS CORRESPONDING TO LOGICAL ADDRESS ARE COMPUTED
S2
SEGMENT MANAGEMENT INFORMATION IN DEFECT MANAGEMENT TABLE IS REFERENCED
S3
YES
DEFECTIVE SECTOR ?
S4
NO
S5
SECTOR IN ALTERNATIVE SEGMENT IS DESIGNATED
RESERVE ALTERNATIVE AREA MANAGEMENT INFORMATION IN DEFECT MANAGEMENT TABLE IS REFERENCED
S6
YES
DEFECTIVE SECTOR ?
S7
S8
SECTOR IN RESERVE ALTERNATIVE AREA IS DESIGNATED
NO
SECTOR IN REGULAR AREA IS DESIGNATED
S9
ACCESS TO DESIGNATED SECTOR
S10
READ DATA/STATUS
RECEPTION
TRANSMISSION
S11
END
END

FIG. 6(A)

CONFIGURATION OF DATA AREA (2096 BYTES)

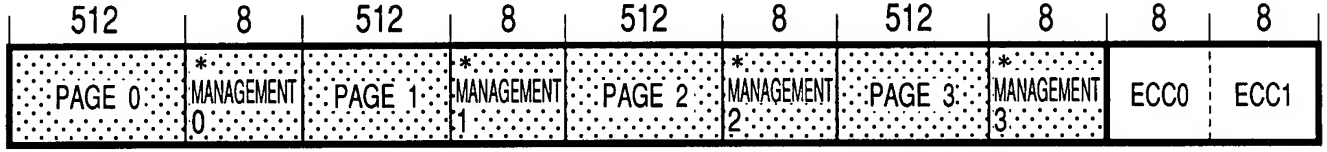


FIG. 6(B)

CONFIGURATION OF SECTOR MANAGEMENT AREA (16 BYTES)

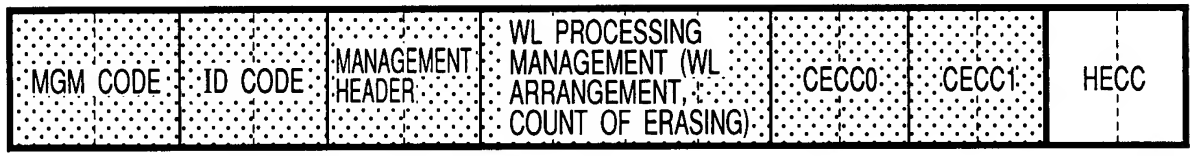


FIG. 6(C)

CONFIGURATION OF SECTOR MANAGEMENT AREA (SAND)

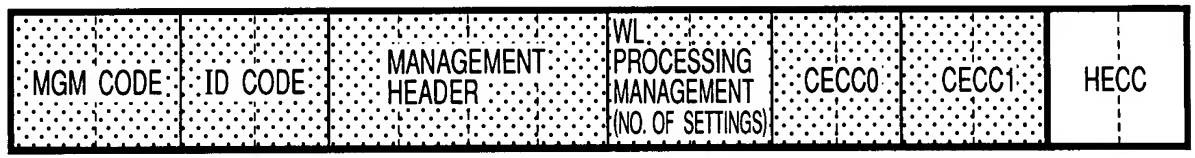


FIG. 7

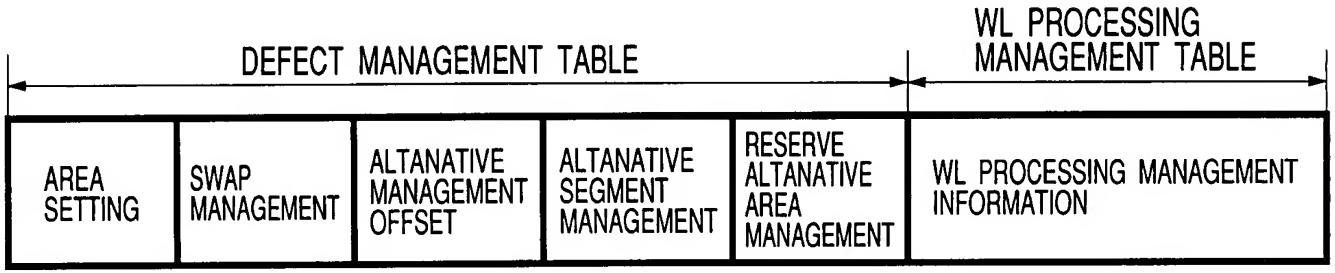


FIG. 8(A)

SWAP MANAGEMENT INFORMATION

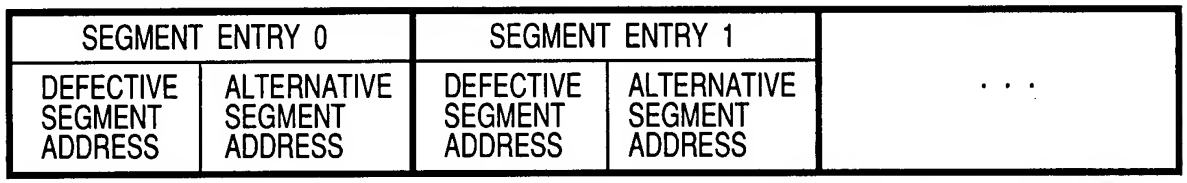


FIG. 8(B)

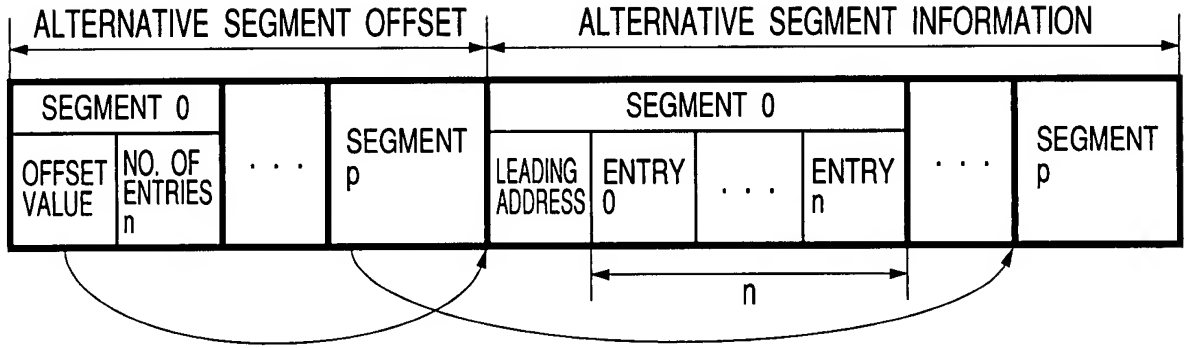


FIG. 8(C)

RESERVE ALTERNATIVE AREA MANAGEMENT INFORMATION

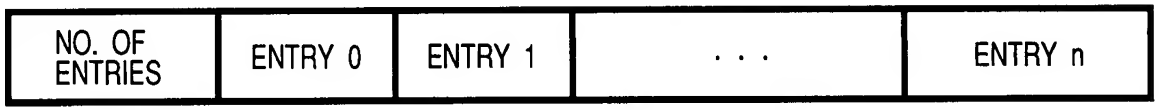


FIG. 8(D)

WL PROCESSING MANAGEMENT INFORMATION

FIG. 9(A) FIG. 9(B) FIG. 9(C)

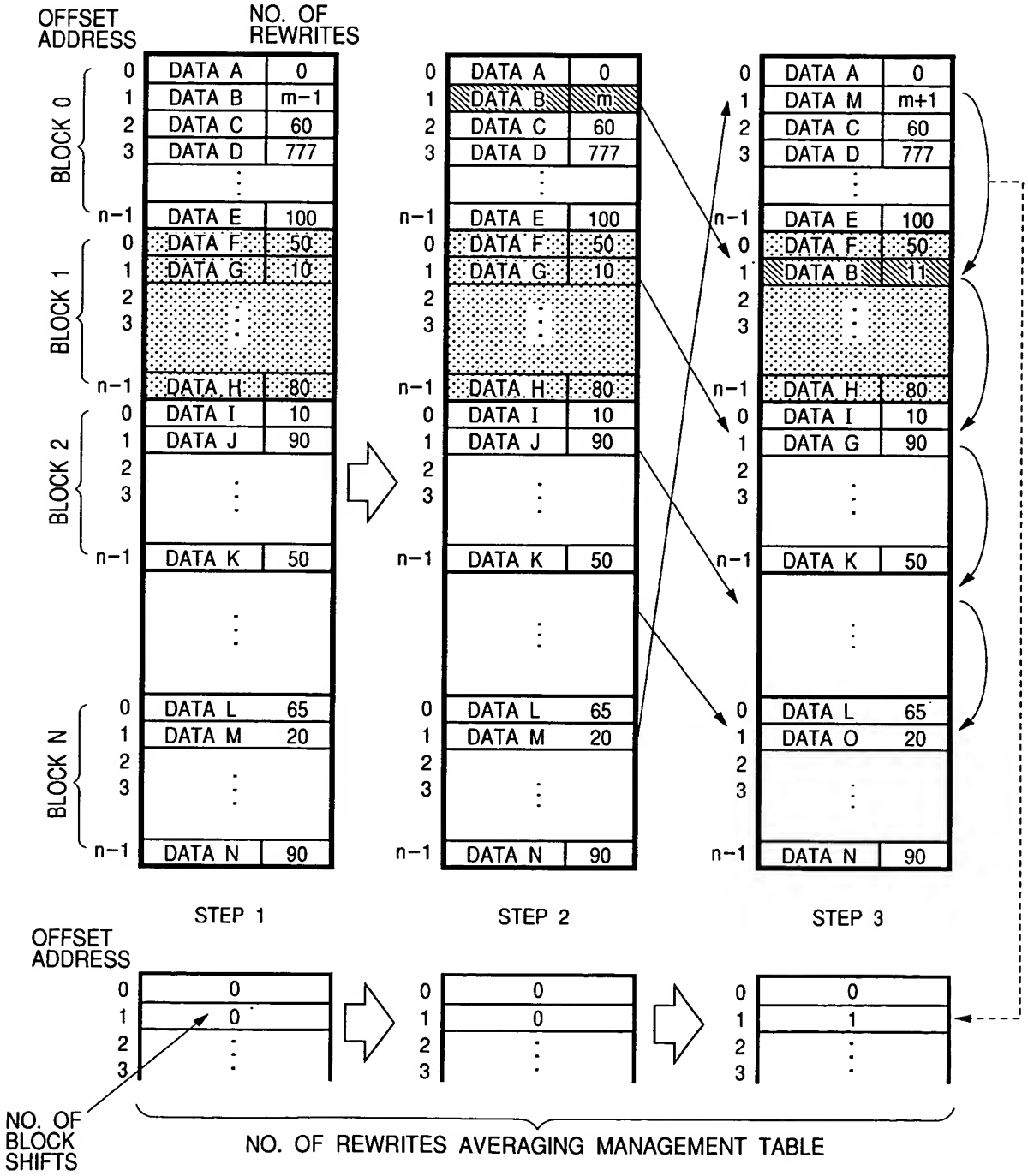


FIG. 10

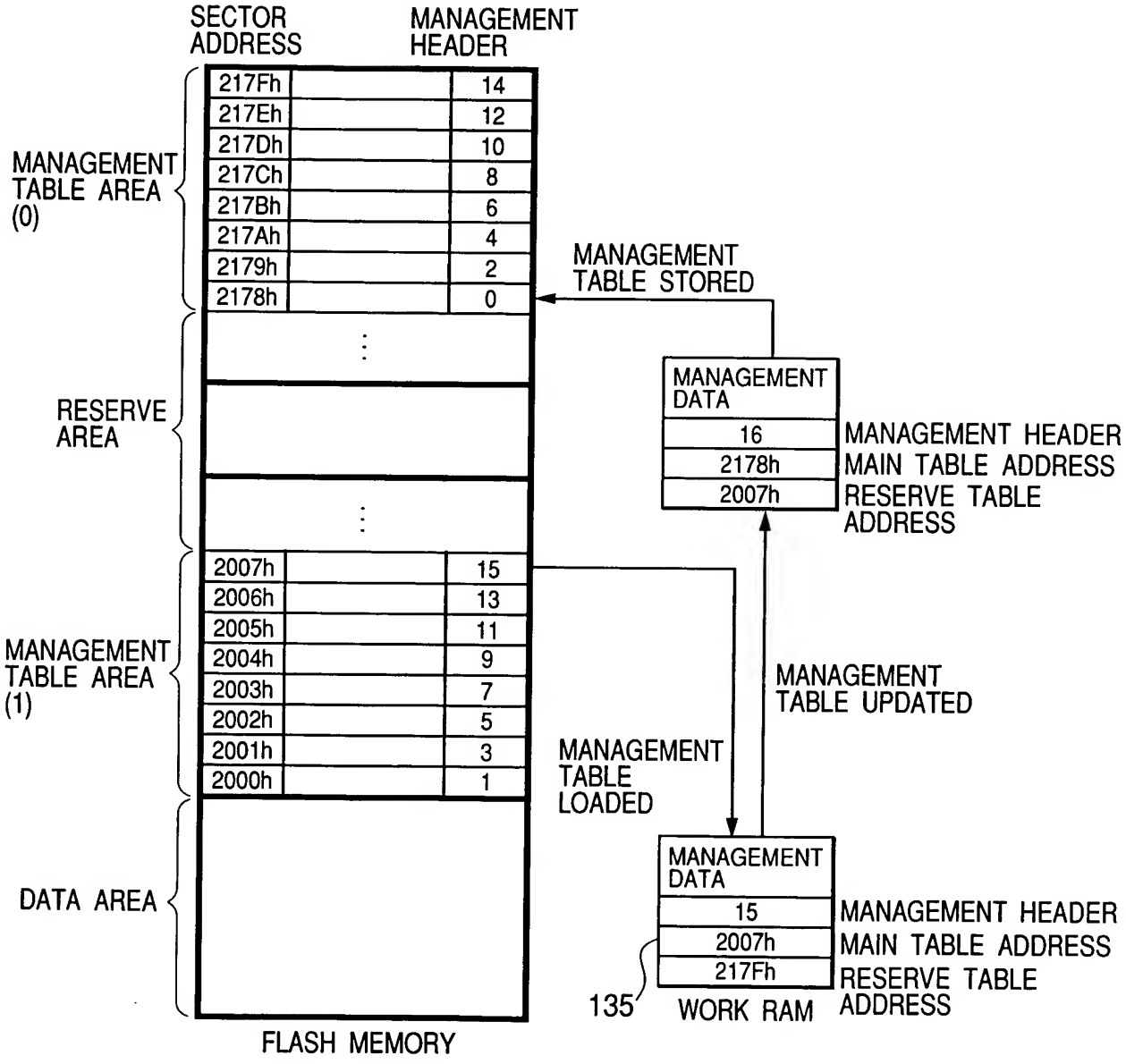

SECTOR ADDRESS
MANAGEMENT HEADER
217Fh
217Eh
217Dh
217Ch
217Bh
217Ah
2179h
2178h
14
12
10
8
6
4
2
0
MANAGEMENT TABLE AREA (0)
RESERVE AREA
2007h
2006h
2005h
2004h
2003h
2002h
2001h
2000h
15
13
11
9
7
5
3
1
MANAGEMENT TABLE AREA (1)
DATA AREA
FLASH MEMORY
MANAGEMENT TABLE STORED
MANAGEMENT TABLE UPDATED
MANAGEMENT TABLE LOADED
MANAGEMENT DATA
16
2178h
2007h
MANAGEMENT HEADER
MAIN TABLE ADDRESS
RESERVE TABLE ADDRESS
MANAGEMENT DATA
15
2007h
217Fh
MANAGEMENT HEADER
MAIN TABLE ADDRESS
RESERVE TABLE ADDRESS
135
WORK RAM

FIG. 11

CONFIGURATION OF WORK RAM (3072 BYTES)

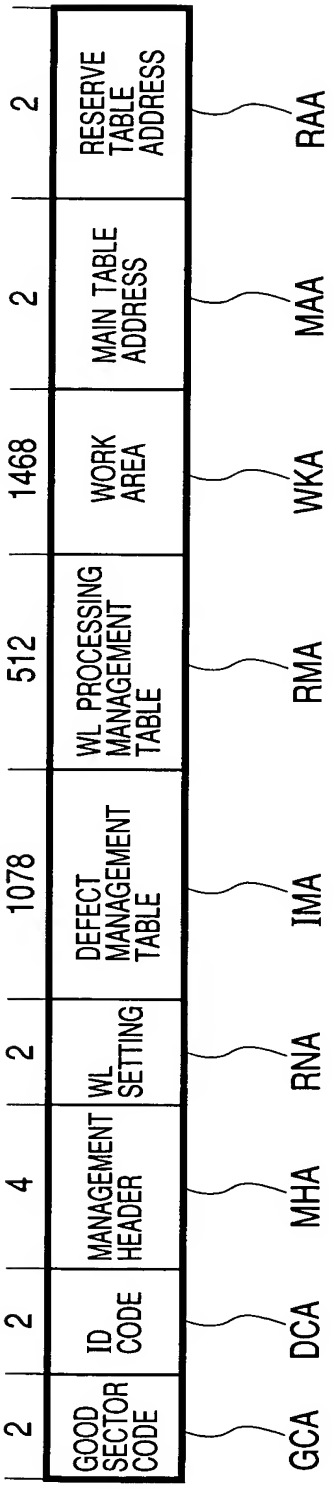


FIG. 12

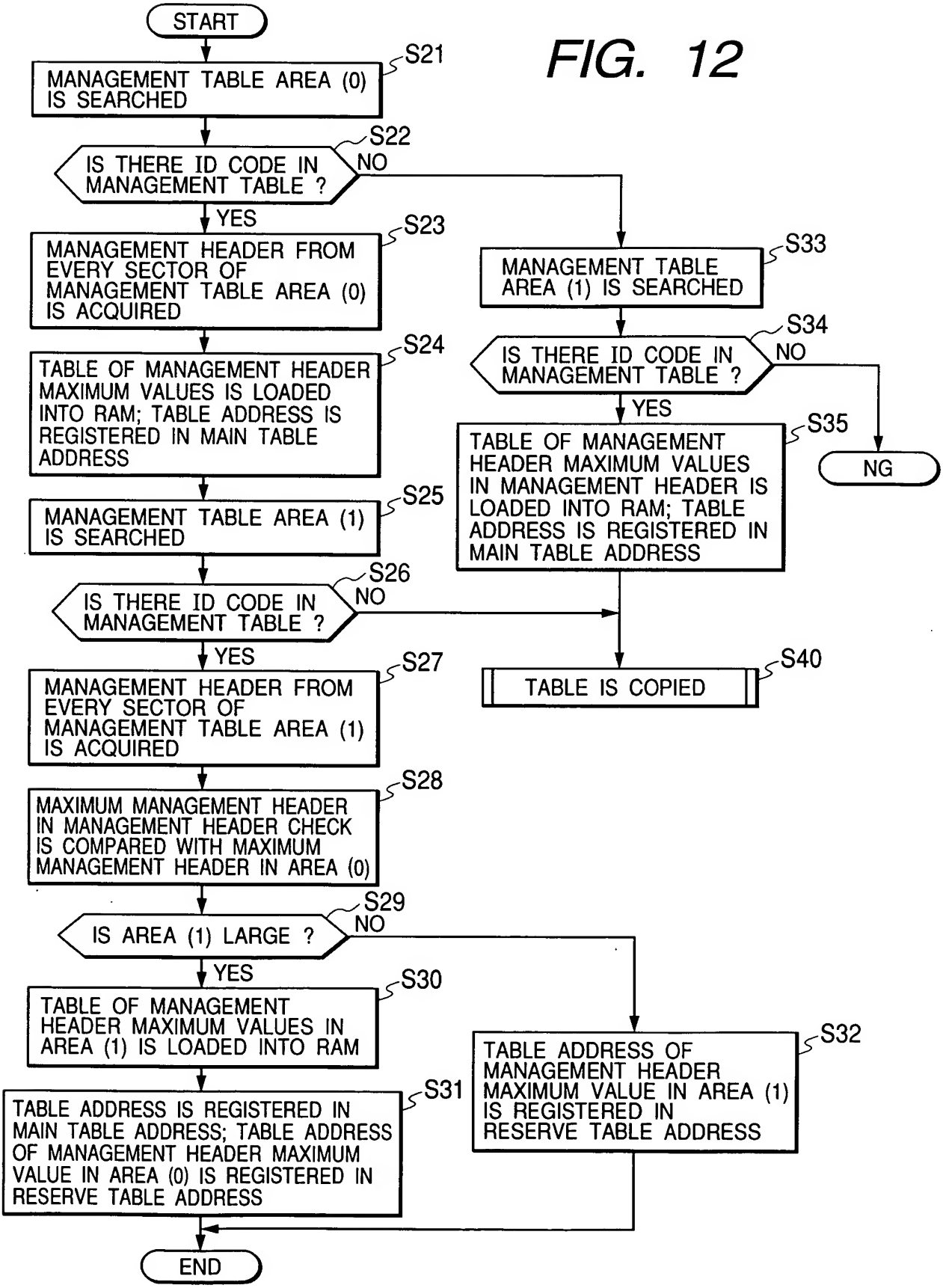

START
MANAGEMENT TABLE AREA (0) IS SEARCHED
S21
IS THERE ID CODE IN MANAGEMENT TABLE ?
S22
NO
YES
MANAGEMENT HEADER FROM EVERY SECTOR OF MANAGEMENT TABLE AREA (0) IS ACQUIRED
S23
TABLE OF MANAGEMENT HEADER MAXIMUM VALUES IS LOADED INTO RAM; TABLE ADDRESS IS REGISTERED IN MAIN TABLE ADDRESS
S24
MANAGEMENT TABLE AREA (1) IS SEARCHED
S25
IS THERE ID CODE IN MANAGEMENT TABLE ?
S26
NO
YES
MANAGEMENT HEADER FROM EVERY SECTOR OF MANAGEMENT TABLE AREA (1) IS ACQUIRED
S27
MAXIMUM MANAGEMENT HEADER IN MANAGEMENT HEADER CHECK IS COMPARED WITH MAXIMUM MANAGEMENT HEADER IN AREA (0)
S28
IS AREA (1) LARGE ?
S29
NO
YES
TABLE OF MANAGEMENT HEADER MAXIMUM VALUES IN AREA (1) IS LOADED INTO RAM
S30
TABLE ADDRESS IS REGISTERED IN MAIN TABLE ADDRESS; TABLE ADDRESS OF MANAGEMENT HEADER MAXIMUM VALUE IN AREA (0) IS REGISTERED IN RESERVE TABLE ADDRESS
S31
TABLE ADDRESS OF MANAGEMENT HEADER MAXIMUM VALUE IN AREA (1) IS REGISTERED IN RESERVE TABLE ADDRESS
S32
END
MANAGEMENT TABLE AREA (1) IS SEARCHED
S33
IS THERE ID CODE IN MANAGEMENT TABLE ?
S34
NO
YES
TABLE OF MANAGEMENT HEADER MAXIMUM VALUES IN MANAGEMENT HEADER IS LOADED INTO RAM; TABLE ADDRESS IS REGISTERED IN MAIN TABLE ADDRESS
S35
NG
TABLE IS COPIED
S40

FIG. 13

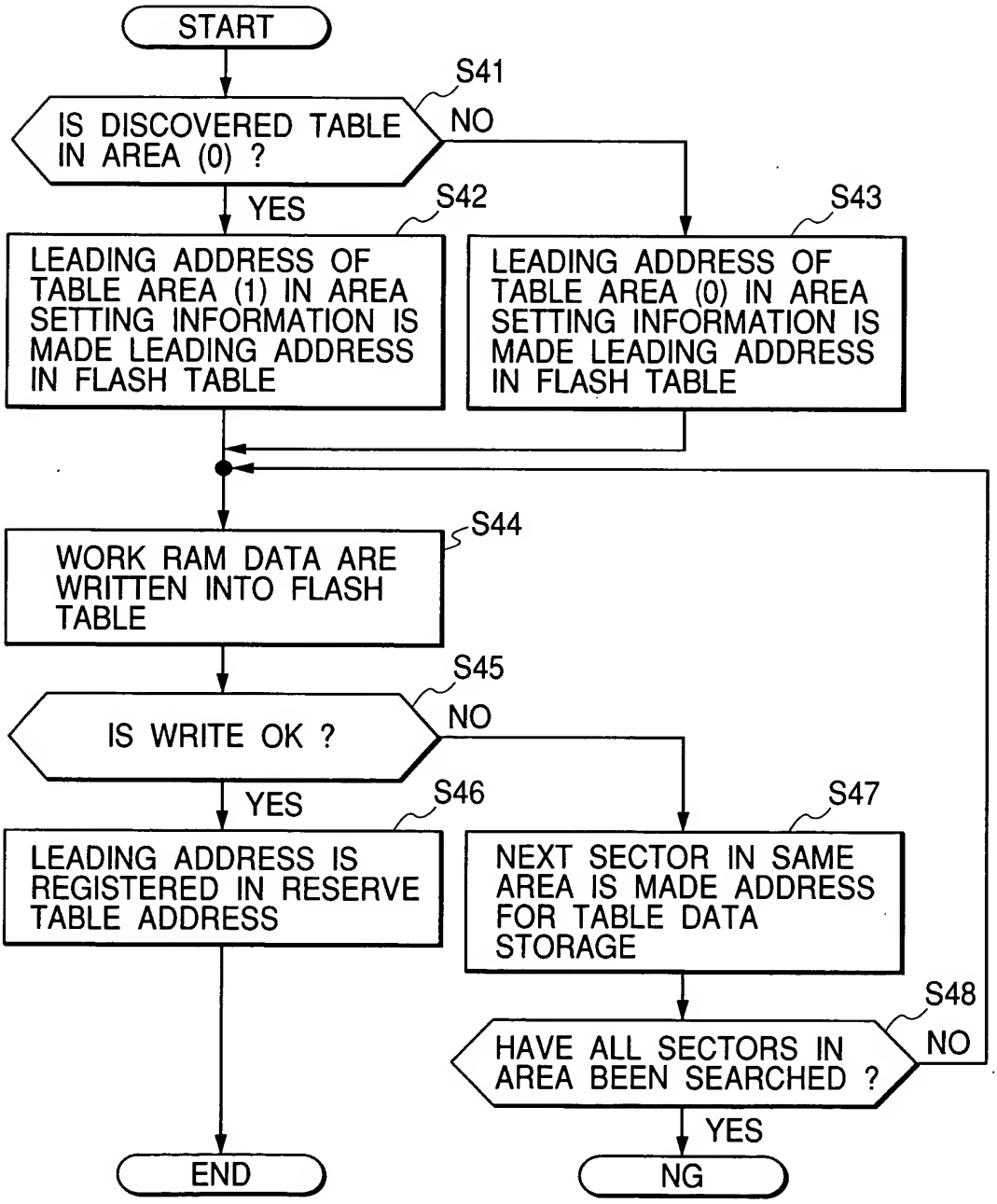

START
S41
IS DISCOVERED TABLE IN AREA (0) ?
NO
YES
S42
LEADING ADDRESS OF TABLE AREA (1) IN AREA SETTING INFORMATION IS MADE LEADING ADDRESS IN FLASH TABLE
S43
LEADING ADDRESS OF TABLE AREA (0) IN AREA SETTING INFORMATION IS MADE LEADING ADDRESS IN FLASH TABLE
S44
WORK RAM DATA ARE WRITTEN INTO FLASH TABLE
S45
IS WRITE OK ?
NO
YES
S46
LEADING ADDRESS IS REGISTERED IN RESERVE TABLE ADDRESS
S47
NEXT SECTOR IN SAME AREA IS MADE ADDRESS FOR TABLE DATA STORAGE
S48
HAVE ALL SECTORS IN AREA BEEN SEARCHED ?
NO
YES
END
NG

FIG. 14

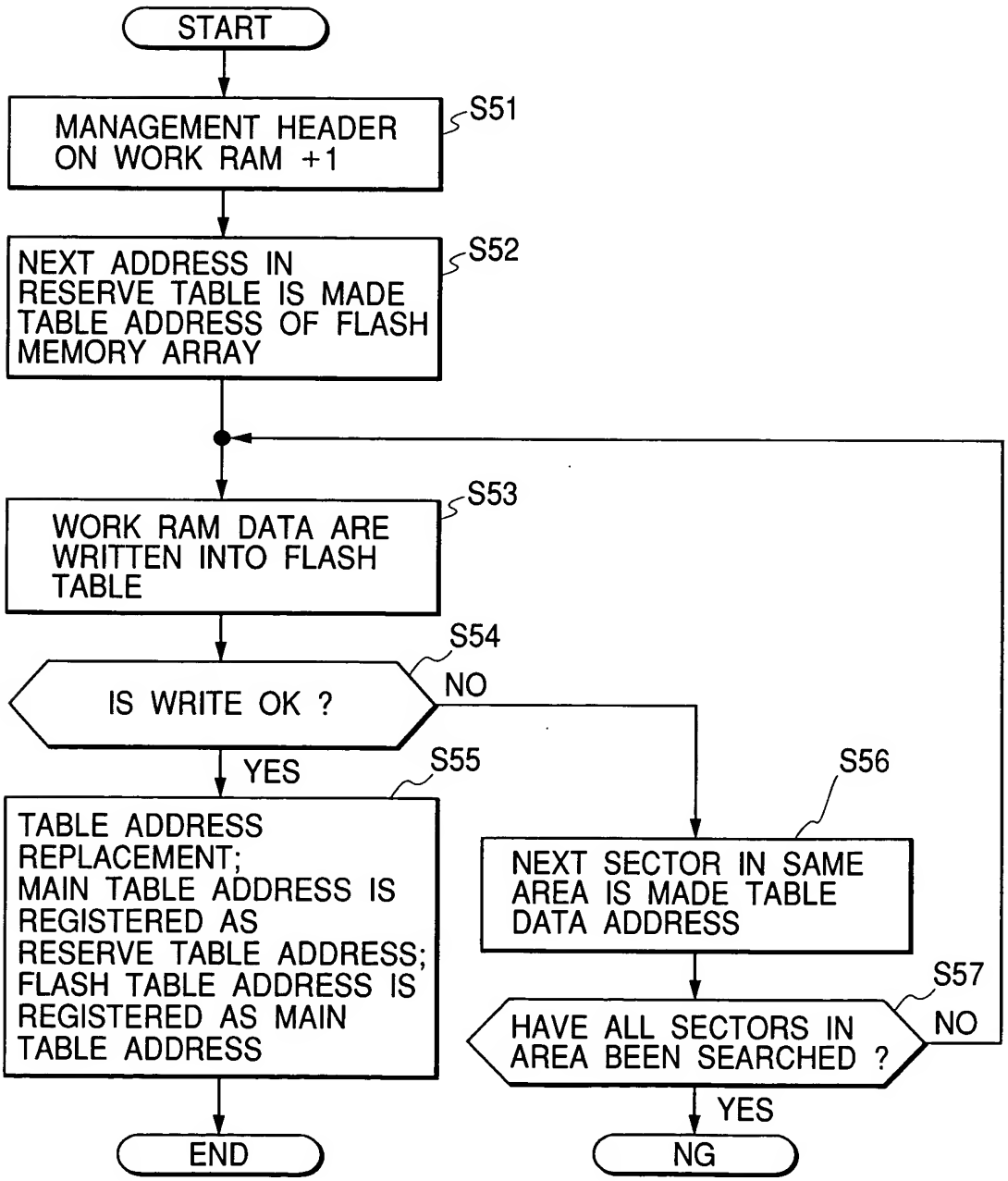

START
MANAGEMENT HEADER ON WORK RAM +1
S51
NEXT ADDRESS IN RESERVE TABLE IS MADE TABLE ADDRESS OF FLASH MEMORY ARRAY
S52
WORK RAM DATA ARE WRITTEN INTO FLASH TABLE
S53
IS WRITE OK ?
S54
NO
YES
TABLE ADDRESS REPLACEMENT; MAIN TABLE ADDRESS IS REGISTERED AS RESERVE TABLE ADDRESS; FLASH TABLE ADDRESS IS REGISTERED AS MAIN TABLE ADDRESS
S55
NEXT SECTOR IN SAME AREA IS MADE TABLE DATA ADDRESS
S56
HAVE ALL SECTORS IN AREA BEEN SEARCHED ?
S57
NO
YES
END
NG

FIG. 15

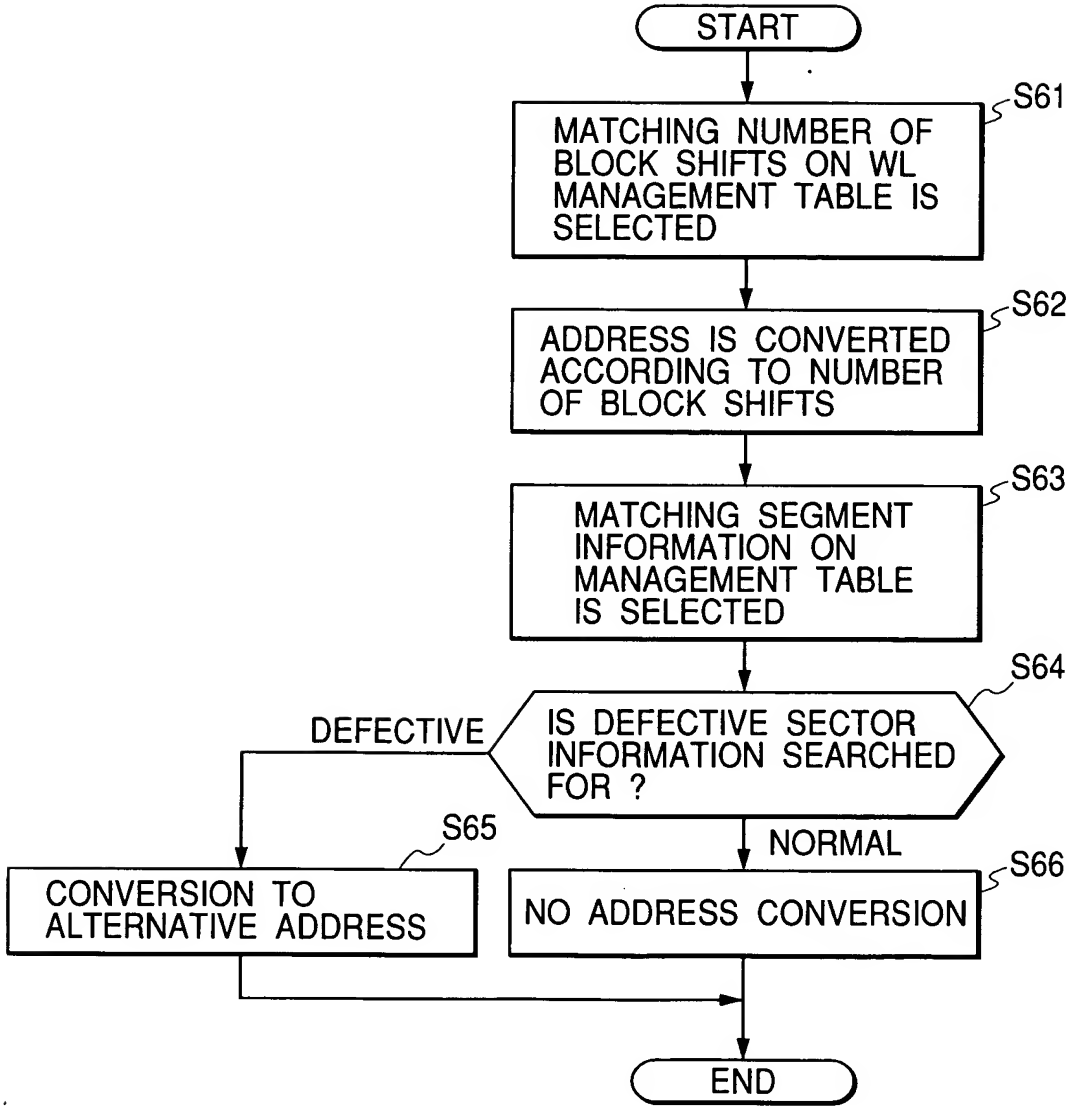

START
S61
MATCHING NUMBER OF BLOCK SHIFTS ON WL MANAGEMENT TABLE IS SELECTED
S62
ADDRESS IS CONVERTED ACCORDING TO NUMBER OF BLOCK SHIFTS
S63
MATCHING SEGMENT INFORMATION ON MANAGEMENT TABLE IS SELECTED
S64
IS DEFECTIVE SECTOR INFORMATION SEARCHED FOR ?
DEFECTIVE
NORMAL
S65
CONVERSION TO ALTERNATIVE ADDRESS
S66
NO ADDRESS CONVERSION
END

FIG. 16

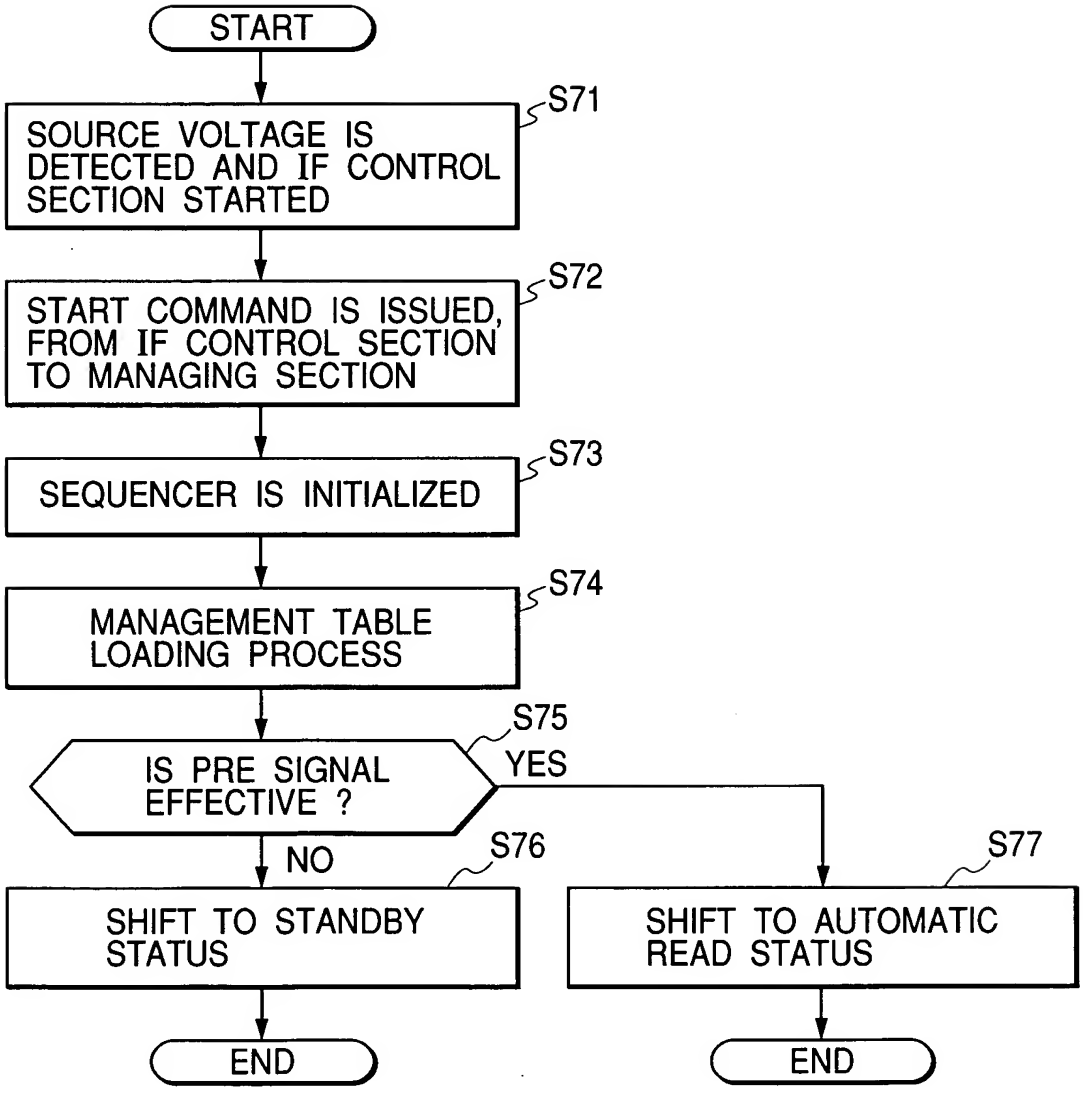

START
SOURCE VOLTAGE IS DETECTED AND IF CONTROL SECTION STARTED
S71
START COMMAND IS ISSUED, FROM IF CONTROL SECTION TO MANAGING SECTION
S72
SEQUENCER IS INITIALIZED
S73
MANAGEMENT TABLE LOADING PROCESS
S74
IS PRE SIGNAL EFFECTIVE ?
S75
YES
NO
S76
SHIFT TO STANDBY STATUS
S77
SHIFT TO AUTOMATIC READ STATUS
END
END

FIG. 17

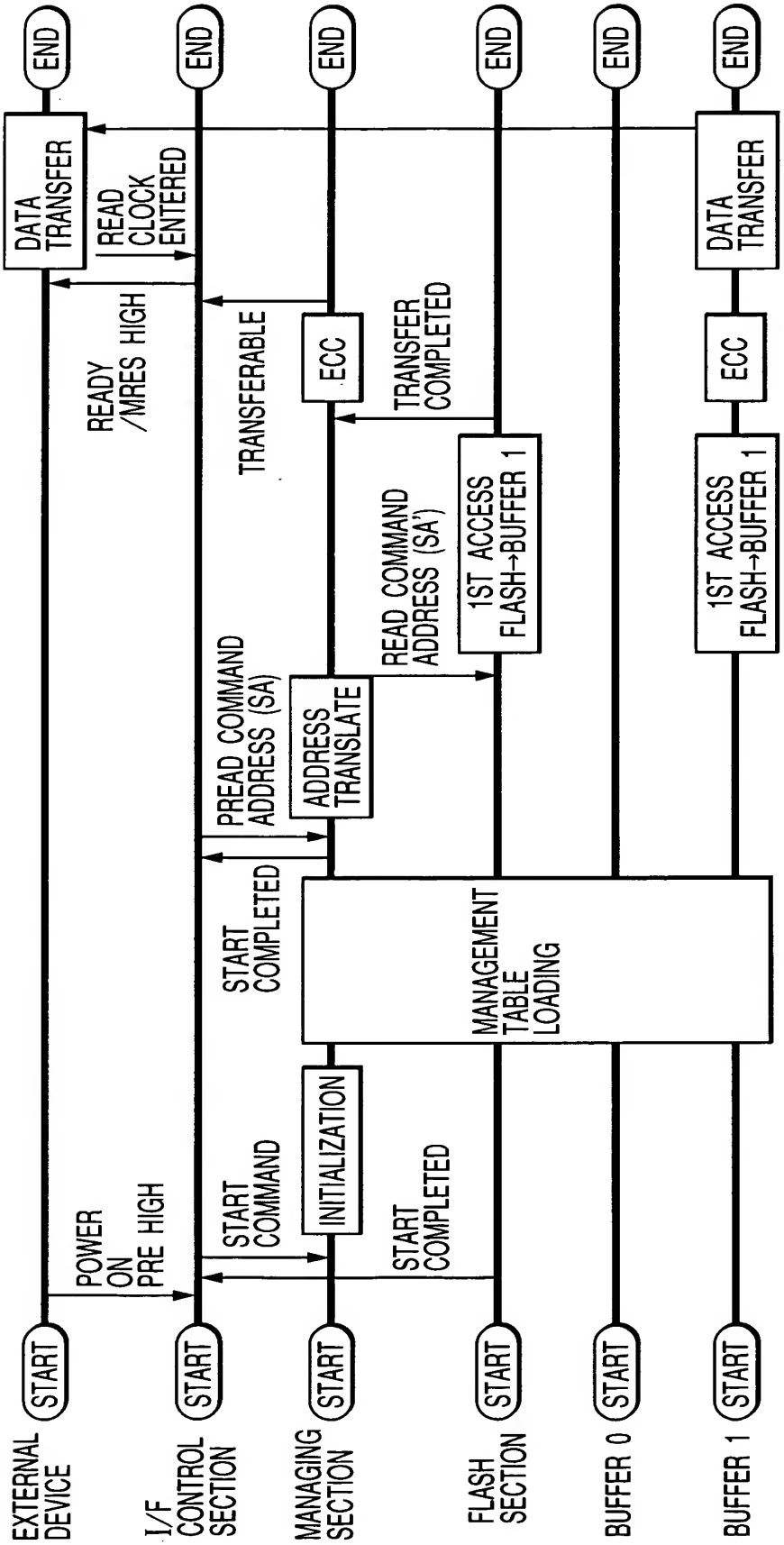

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
END
POWER ON PRE HIGH
START COMMAND
INITIALIZATION
START COMPLETED
READY /MRES HIGH
READ CLOCK ENTERED
DATA TRANSFER
PREAD COMMAND ADDRESS (SA)
ADDRESS TRANSLATE
START COMPLETED
TRANSFERABLE
READ COMMAND ADDRESS (SA')
1ST ACCESS FLASH→BUFFER 1
ECC
TRANSFER COMPLETED
MANAGEMENT TABLE LOADING
1ST ACCESS FLASH→BUFFER 1
ECC
DATA TRANSFER

FIG. 18

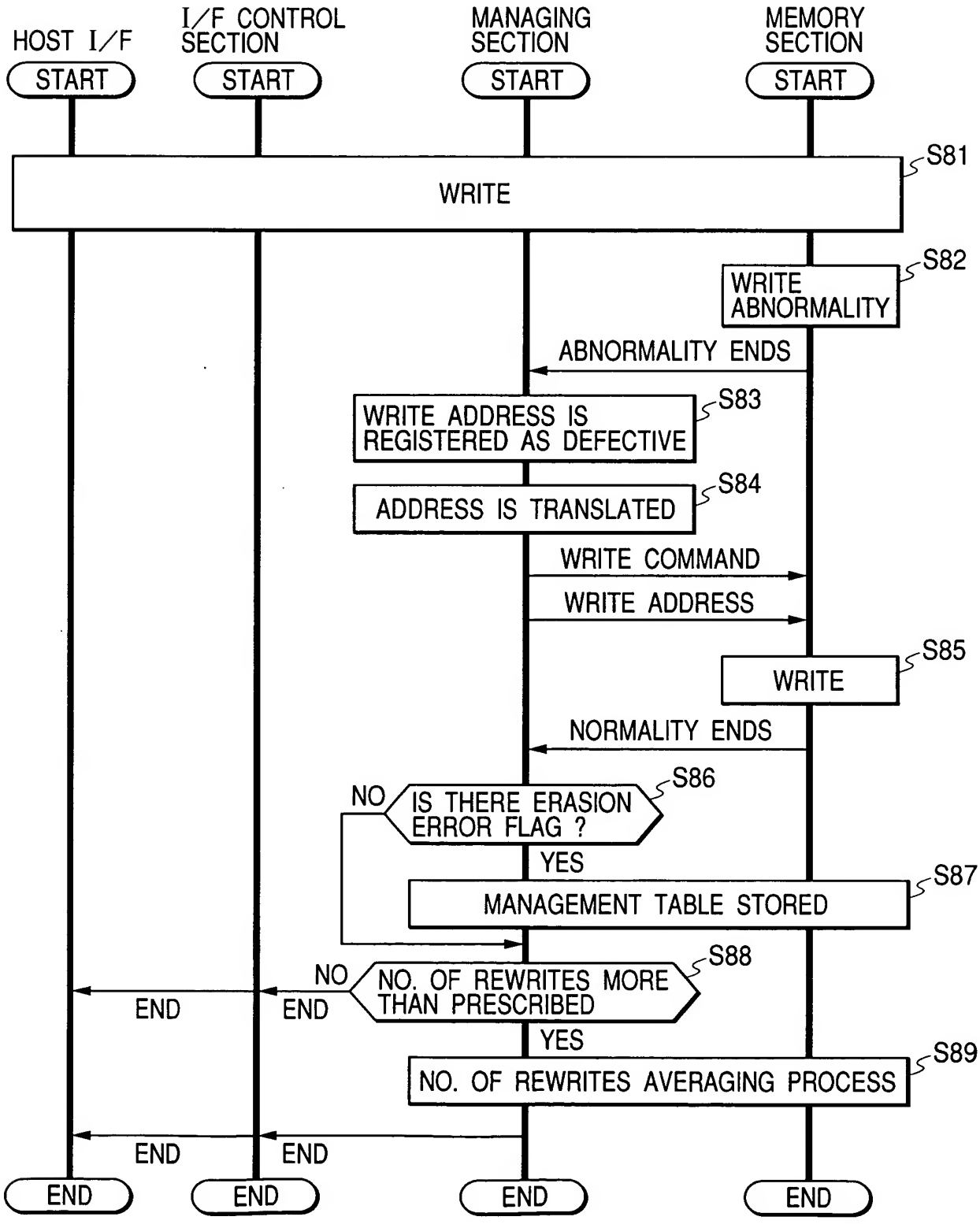

HOST I/F
I/F CONTROL SECTION
MANAGING SECTION
MEMORY SECTION
START
START
START
START
S81
WRITE
S82
WRITE ABNORMALITY
ABNORMALITY ENDS
S83
WRITE ADDRESS IS REGISTERED AS DEFECTIVE
S84
ADDRESS IS TRANSLATED
WRITE COMMAND
WRITE ADDRESS
S85
WRITE
NORMALITY ENDS
S86
NO
IS THERE ERASION ERROR FLAG ?
YES
S87
MANAGEMENT TABLE STORED
S88
NO
NO. OF REWRITES MORE THAN PRESCRIBED
END
END
YES
S89
NO. OF REWRITES AVERAGING PROCESS
END
END
END
END
END

FIG. 19

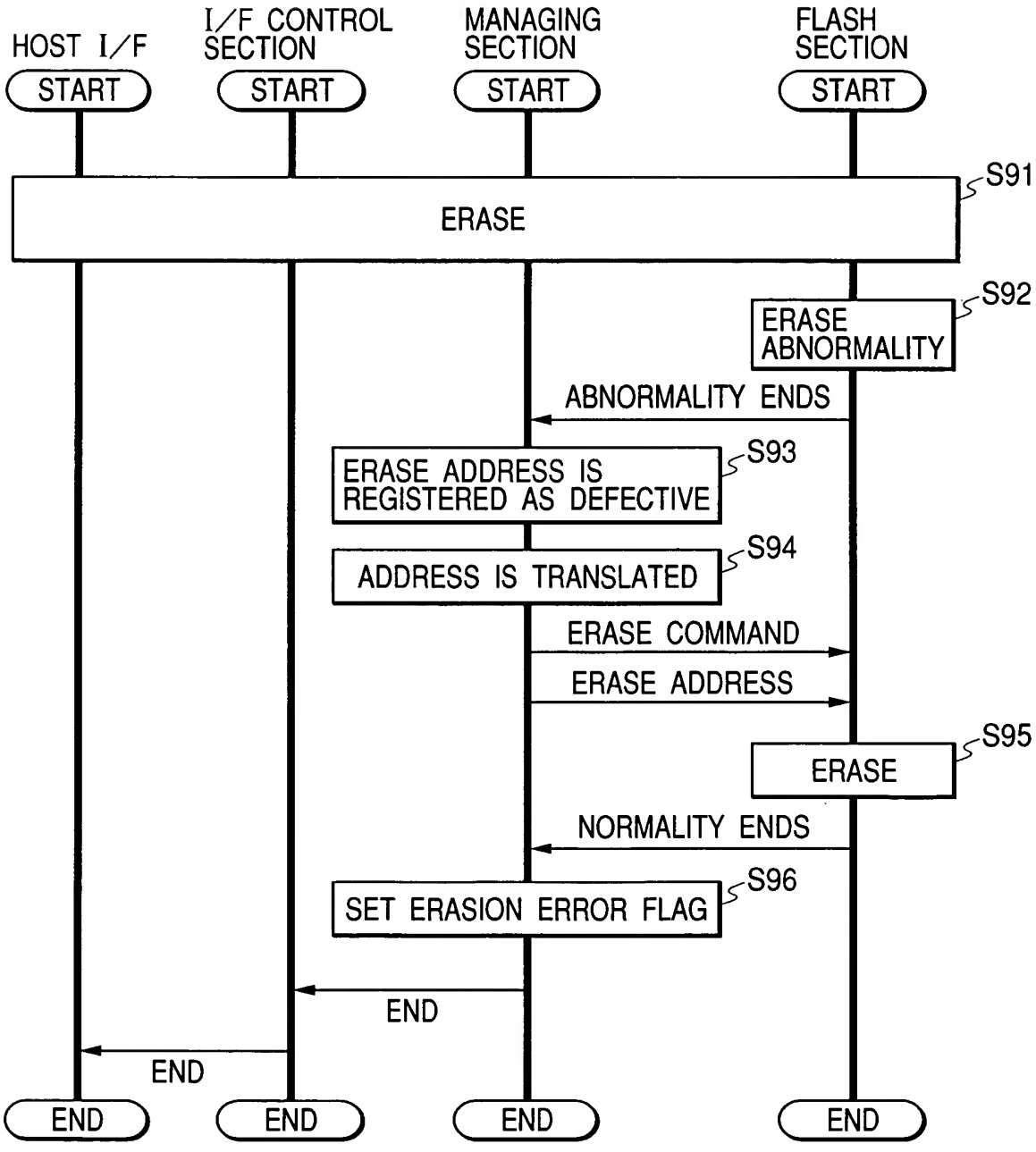

HOST I/F
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
START
START
START
START
S91
ERASE
S92
ERASE ABNORMALITY
ABNORMALITY ENDS
S93
ERASE ADDRESS IS REGISTERED AS DEFECTIVE
S94
ADDRESS IS TRANSLATED
ERASE COMMAND
ERASE ADDRESS
S95
ERASE
NORMALITY ENDS
S96
SET ERASION ERROR FLAG
END
END
END
END
END
END

FIG. 20

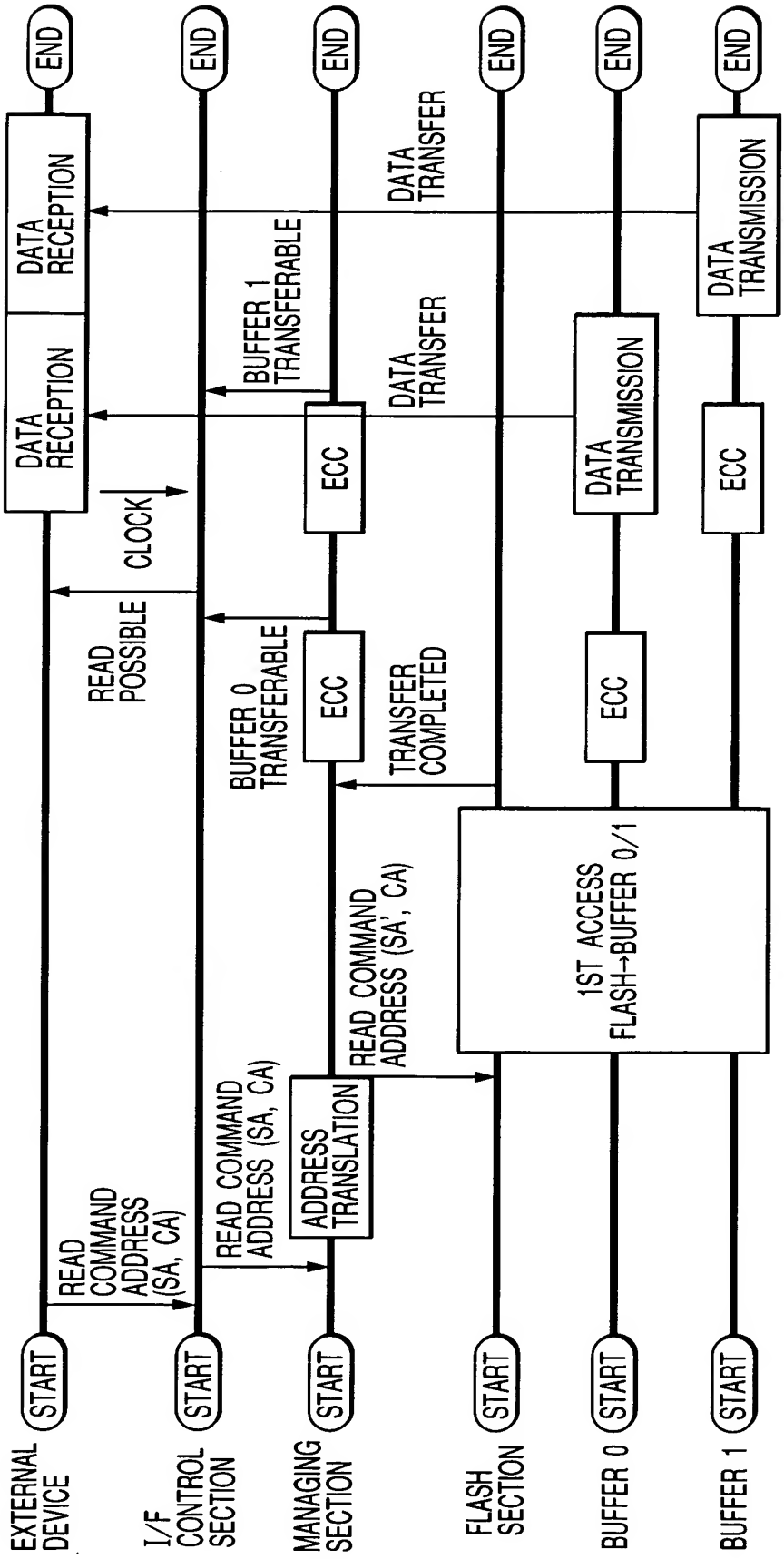

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
END
READ COMMAND ADDRESS (SA, CA)
READ POSSIBLE
CLOCK
DATA RECEPTION
DATA RECEPTION
ADDRESS TRANSLATION
READ COMMAND ADDRESS (SA, CA)
BUFFER 0 TRANSFERABLE
ECC
BUFFER 1 TRANSFERABLE
ECC
READ COMMAND ADDRESS (SA', CA)
TRANSFER COMPLETED
1ST ACCESS FLASH→BUFFER 0/1
DATA TRANSFER
DATA TRANSFER
DATA TRANSFER
DATA TRANSMISSION
ECC
DATA TRANSMISSION

FIG. 21

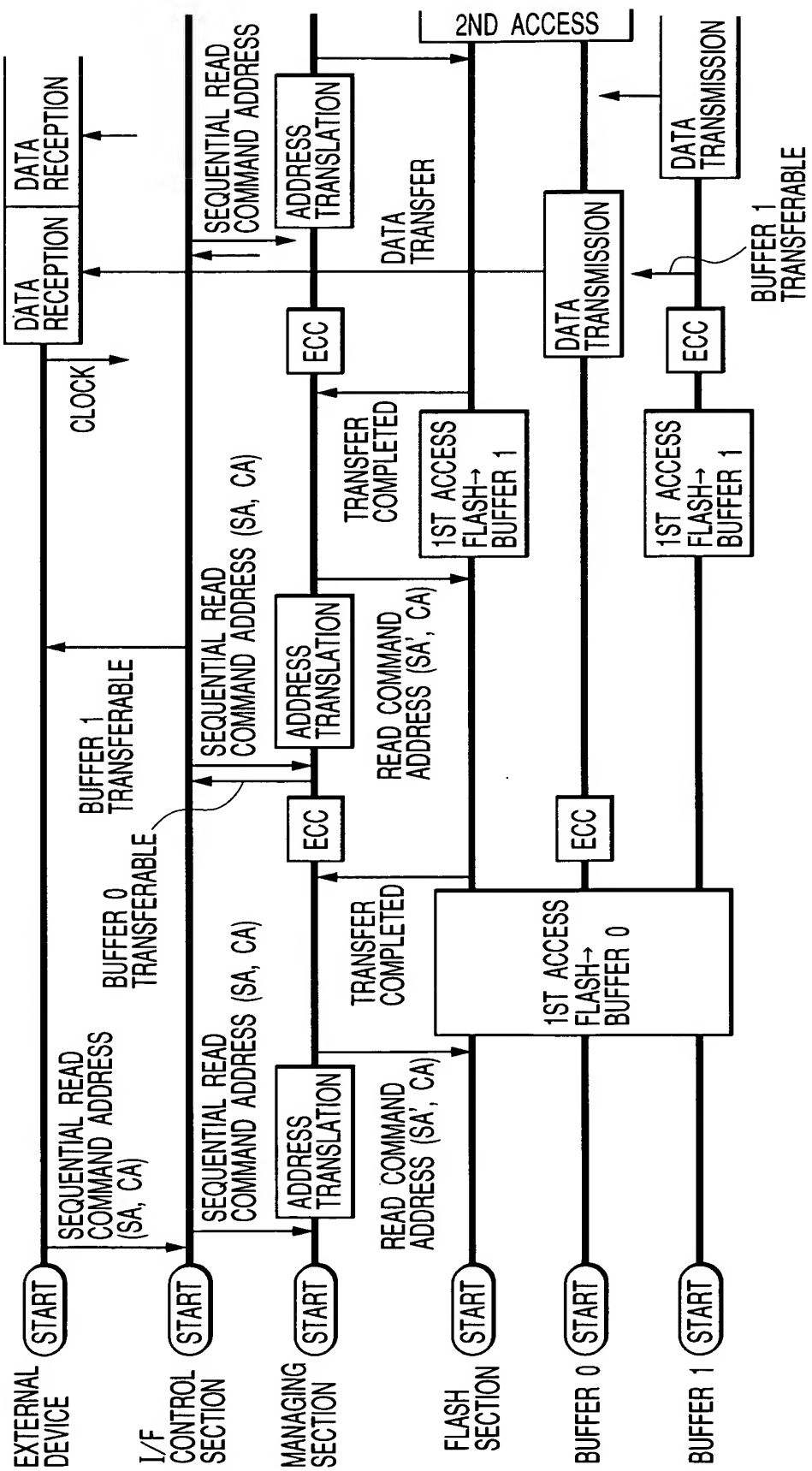

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
SEQUENTIAL READ COMMAND ADDRESS (SA, CA)
BUFFER 0 TRANSFERABLE
BUFFER 1 TRANSFERABLE
CLOCK
DATA RECEPTION
DATA TRANSMISSION
ADDRESS TRANSLATION
ECC
READ COMMAND ADDRESS (SA', CA)
TRANSFER COMPLETED
1ST ACCESS FLASH→ BUFFER 0
1ST ACCESS FLASH→ BUFFER 1
DATA TRANSFER
2ND ACCESS

FIG. 22

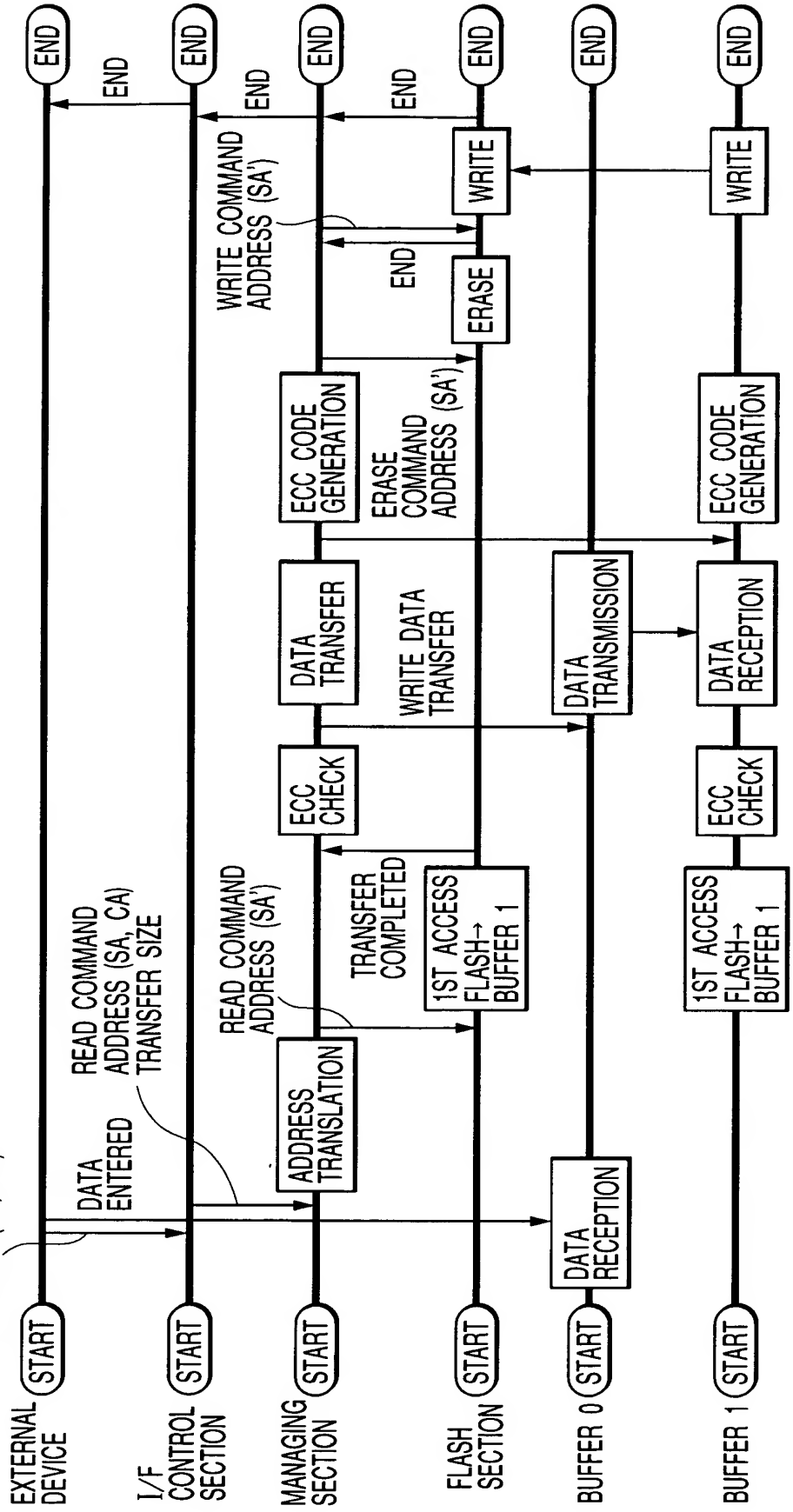

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
END
REWRITE COMMAND ADDRESS (SA, CA)
DATA ENTERED
READ COMMAND ADDRESS (SA, CA) TRANSFER SIZE
ADDRESS TRANSLATION
READ COMMAND ADDRESS (SA')
1ST ACCESS FLASH→ BUFFER 1
TRANSFER COMPLETED
ECC CHECK
DATA TRANSFER
ECC CODE GENERATION
WRITE COMMAND ADDRESS (SA')
ERASE
ERASE COMMAND ADDRESS (SA')
WRITE DATA TRANSFER
WRITE
DATA RECEPTION
DATA TRANSMISSION
DATA RECEPTION
ECC CHECK
1ST ACCESS FLASH→ BUFFER 1
ECC CODE GENERATION
WRITE

FIG. 23

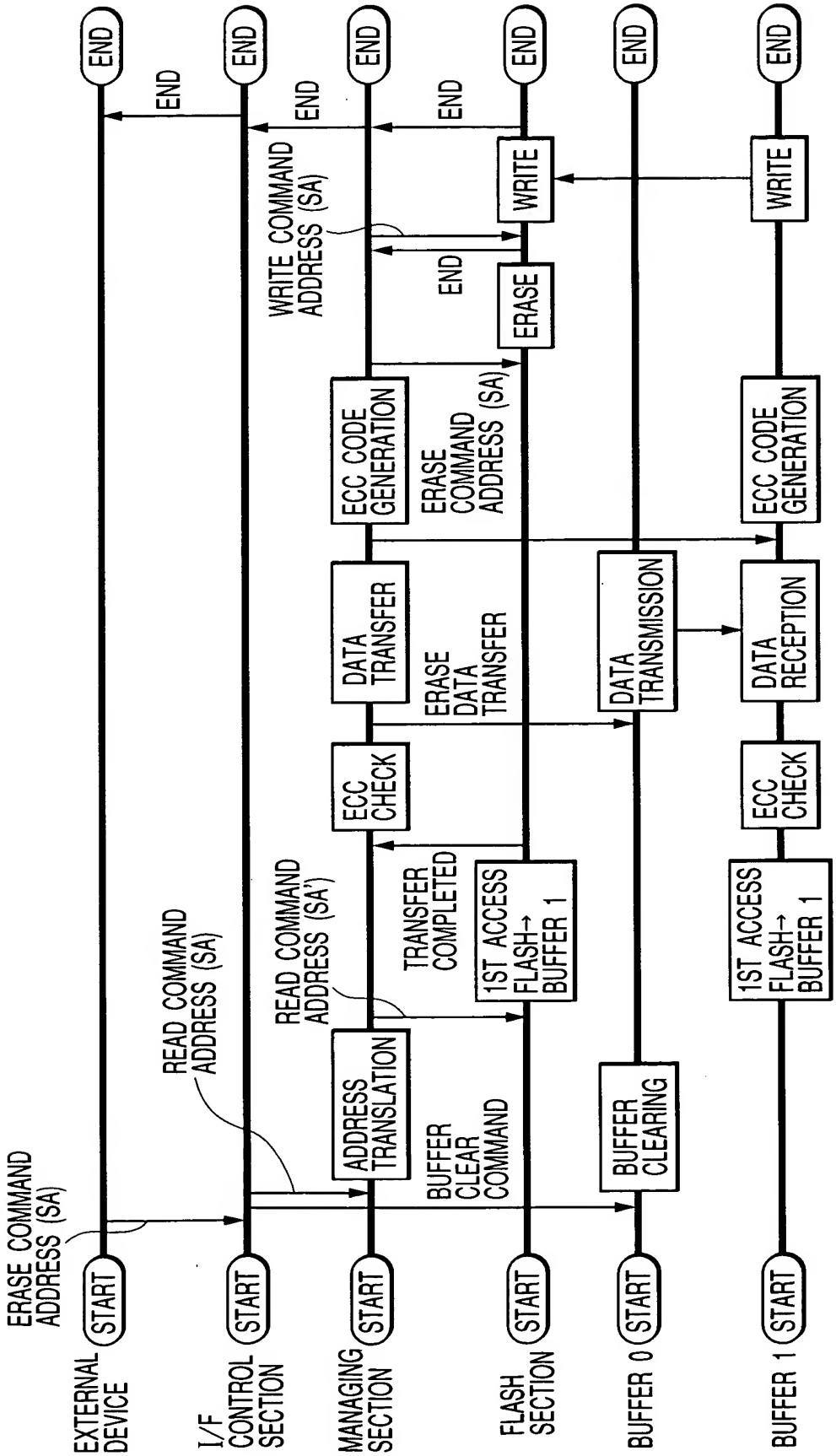

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
END
ERASE COMMAND ADDRESS (SA)
READ COMMAND ADDRESS (SA)
READ COMMAND ADDRESS (SA')
WRITE COMMAND ADDRESS (SA)
ADDRESS TRANSLATION
BUFFER CLEAR COMMAND
TRANSFER COMPLETED
1ST ACCESS FLASH→ BUFFER 1
ECC CHECK
DATA TRANSFER
ERASE DATA TRANSFER
ECC CODE GENERATION
ERASE COMMAND ADDRESS (SA)
ERASE
WRITE
BUFFER CLEARING
DATA TRANSMISSION
1ST ACCESS FLASH→ BUFFER 1
ECC CHECK
DATA RECEPTION
ECC CODE GENERATION
WRITE

FIG. 24

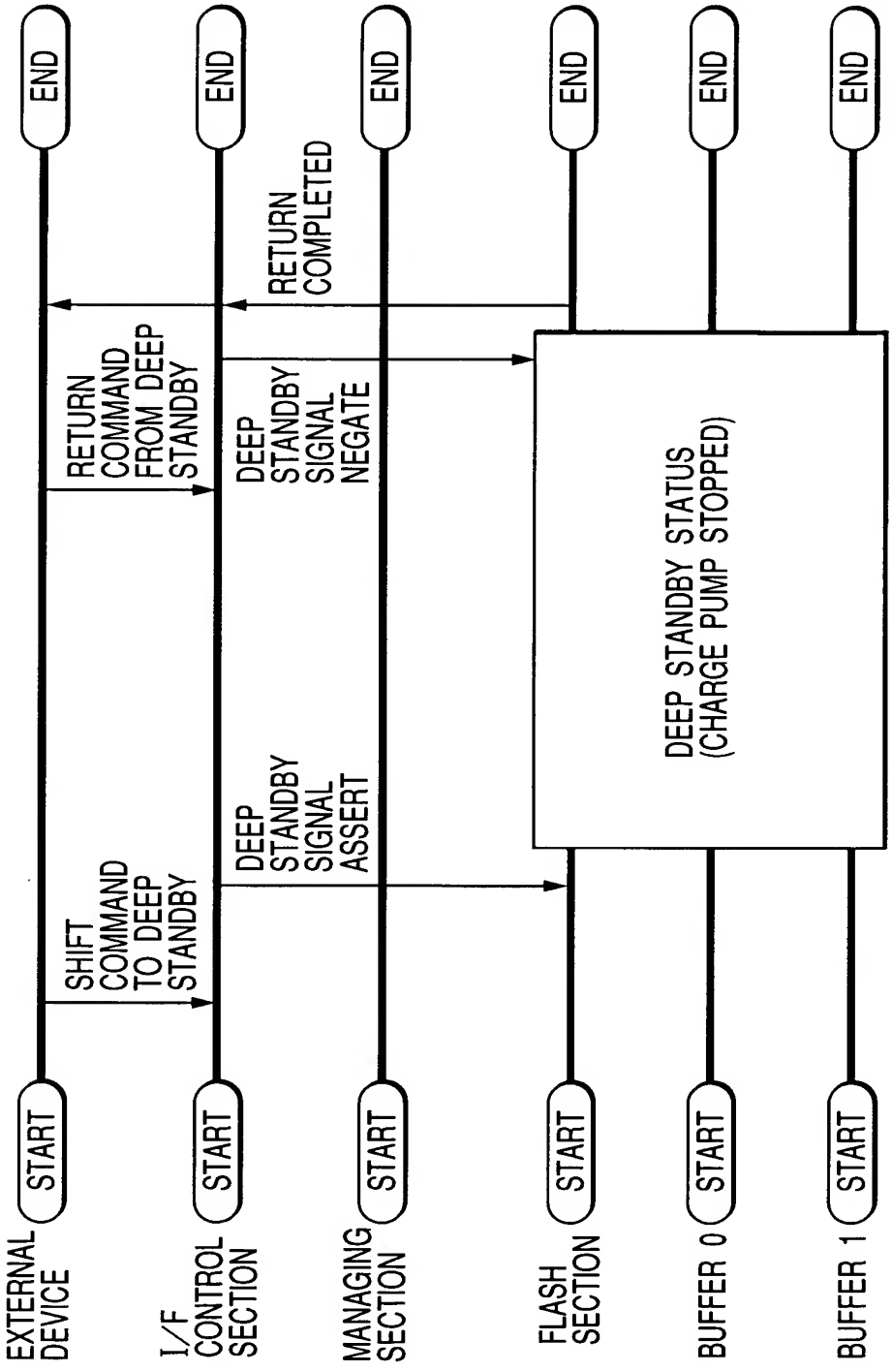

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
END
SHIFT COMMAND TO DEEP STANDBY
RETURN COMMAND FROM DEEP STANDBY
DEEP STANDBY SIGNAL ASSERT
DEEP STANDBY SIGNAL NEGATE
RETURN COMPLETED
DEEP STANDBY STATUS (CHARGE PUMP STOPPED)

FIG. 25

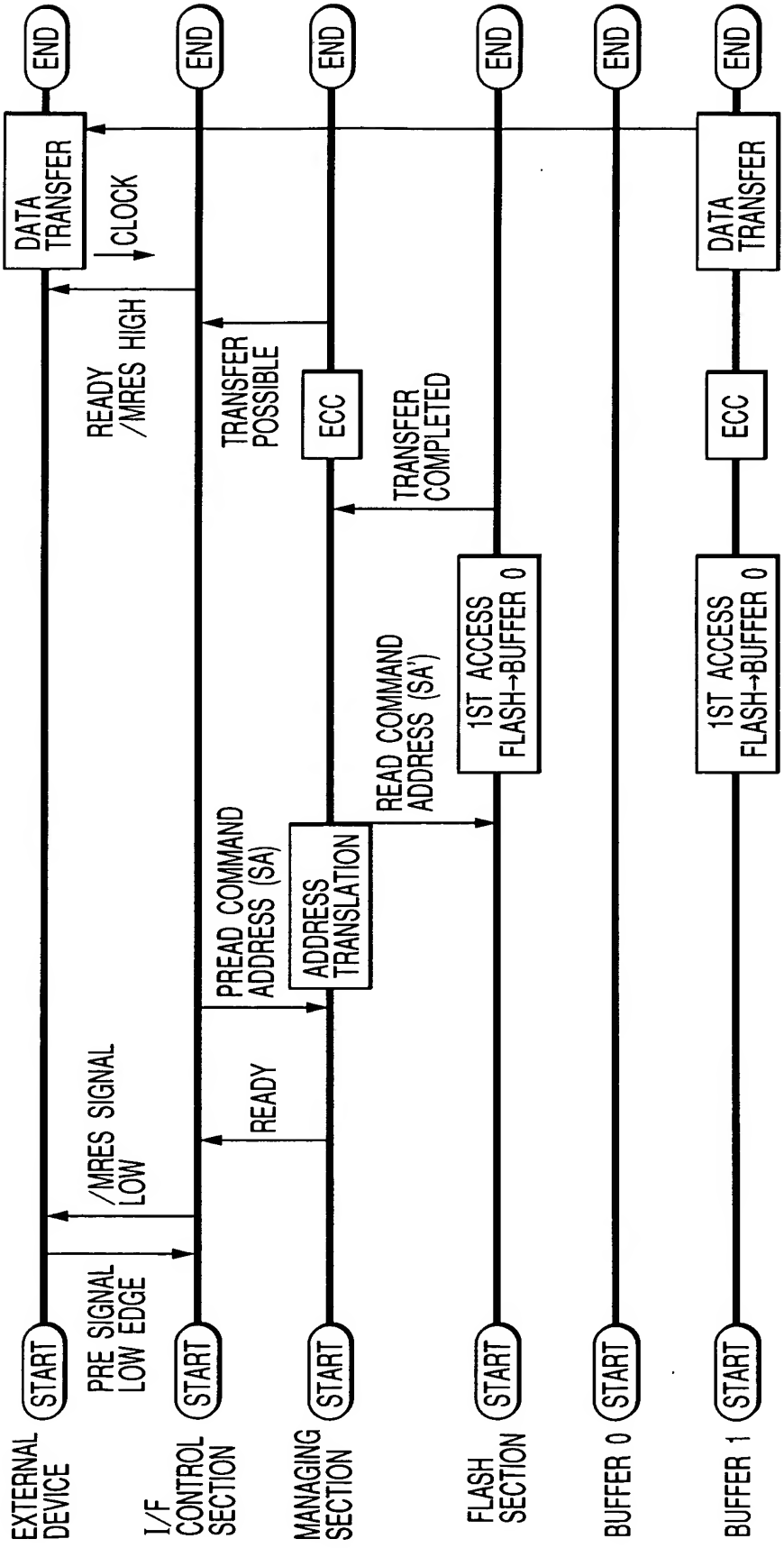

EXTERNAL DEVICE
I/F CONTROL SECTION
MANAGING SECTION
FLASH SECTION
BUFFER 0
BUFFER 1
START
END
PRE SIGNAL LOW EDGE
/MRES SIGNAL LOW
READY
PREAD COMMAND ADDRESS (SA)
ADDRESS TRANSLATION
READ COMMAND ADDRESS (SA')
1ST ACCESS FLASH→BUFFER 0
TRANSFER COMPLETED
ECC
TRANSFER POSSIBLE
READY /MRES HIGH
CLOCK
DATA TRANSFER

FIG. 26

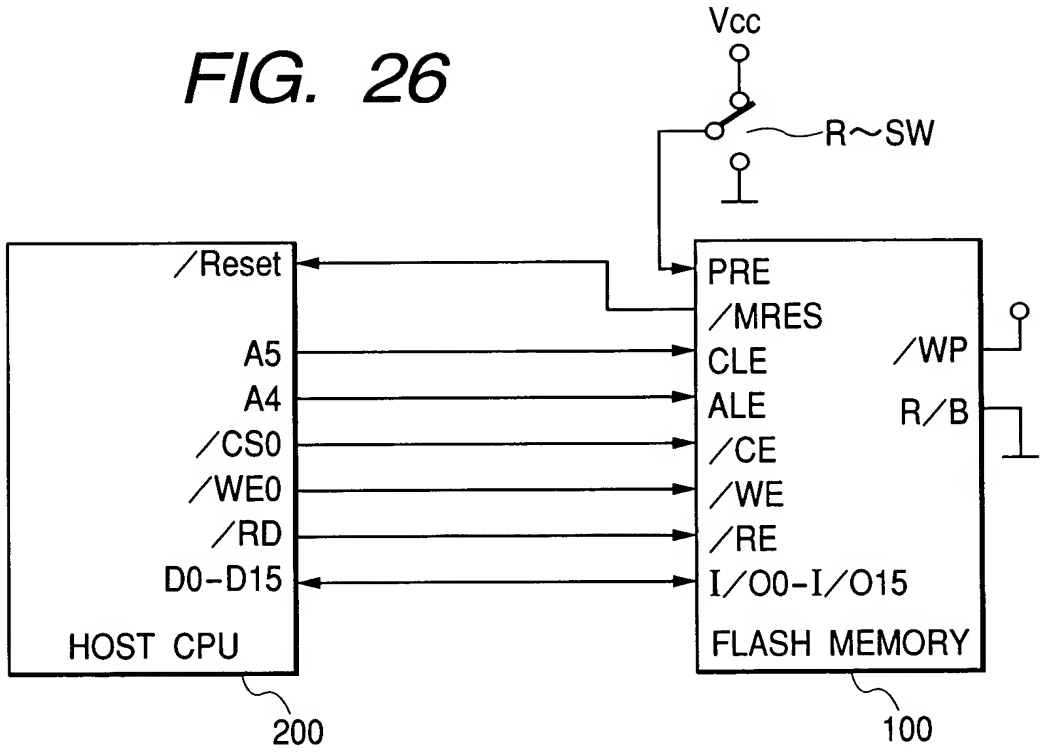


FIG. 27(A)

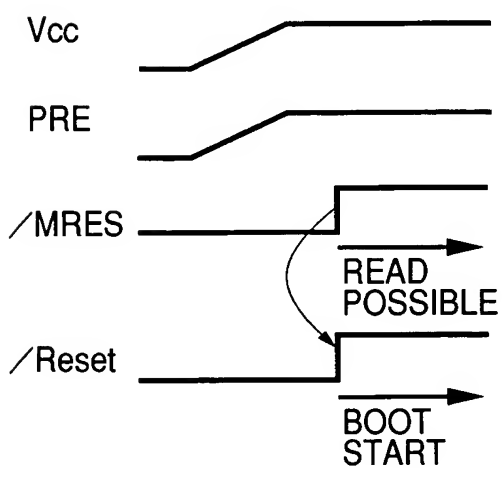


FIG. 27(B)

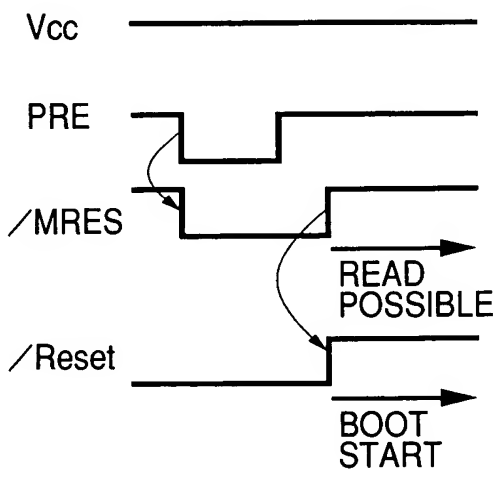


FIG. 28(A)

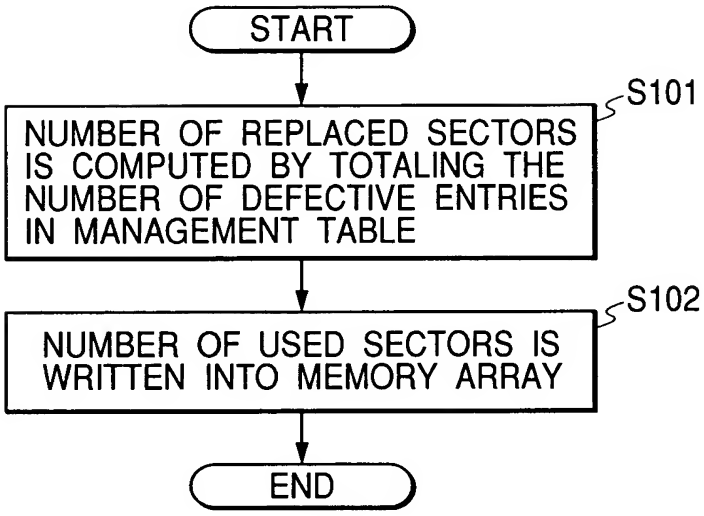


FIG. 28(B)

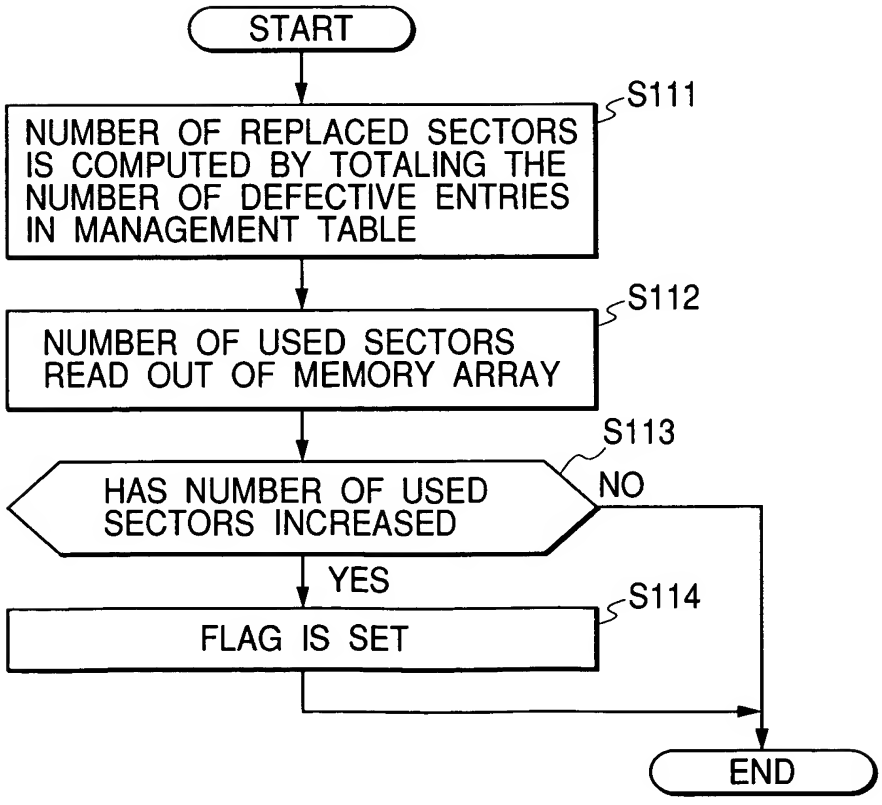
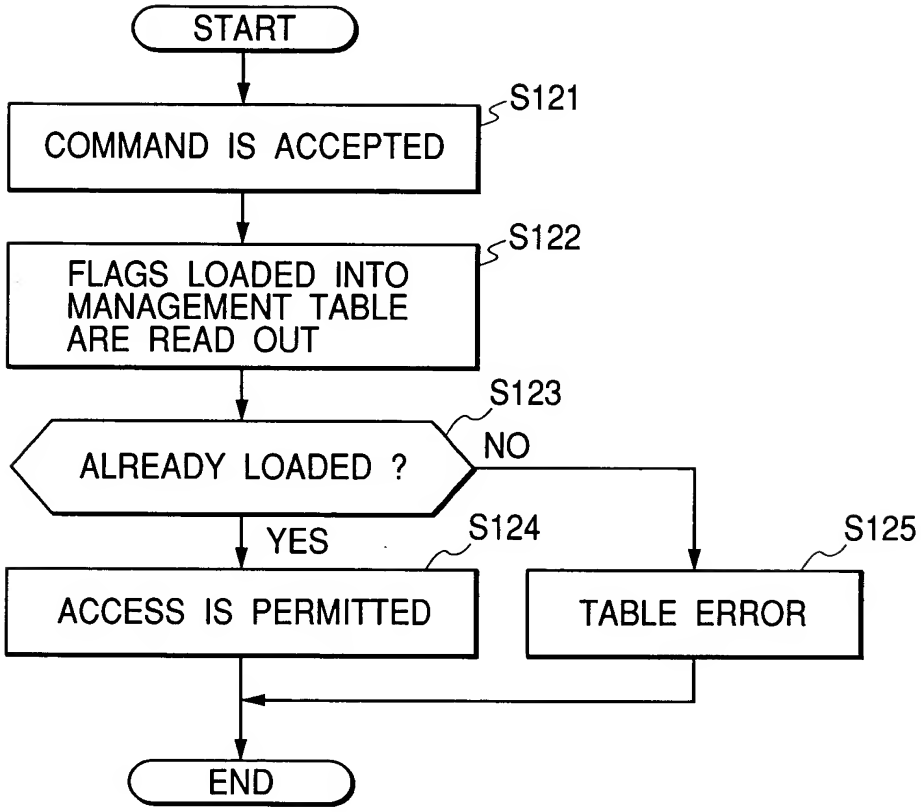


FIG. 29


START
S121
COMMAND IS ACCEPTED
S122
FLAGS LOADED INTO MANAGEMENT TABLE ARE READ OUT
S123
ALREADY LOADED ?
NO
YES
S124
ACCESS IS PERMITTED
S125
TABLE ERROR
END